



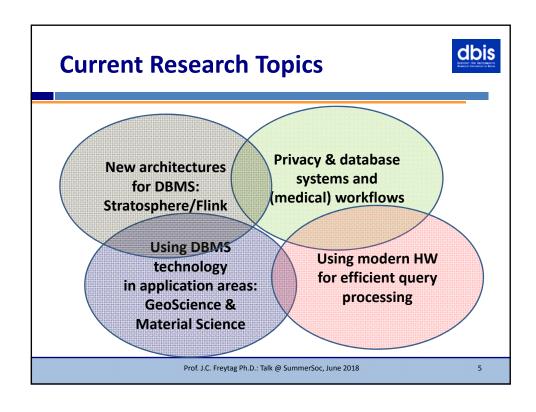
Challenges for data intensive services by recent hardware developments

Prof. Johann Christoph Freytag, Ph.D.
Institut für Informatik, Humboldt-Universität zu Berlin
Mainly based on PhD thesis by Steffen Zeuch (April 2018)

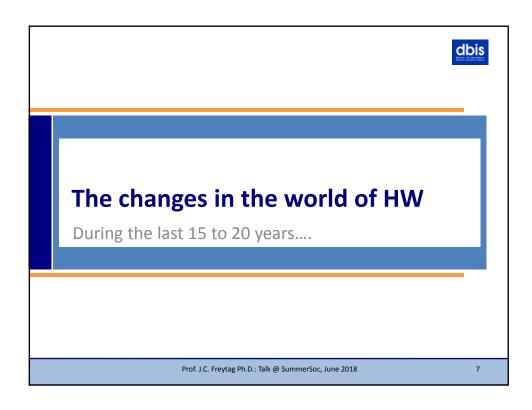
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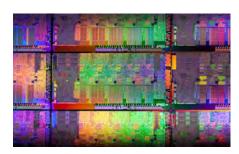




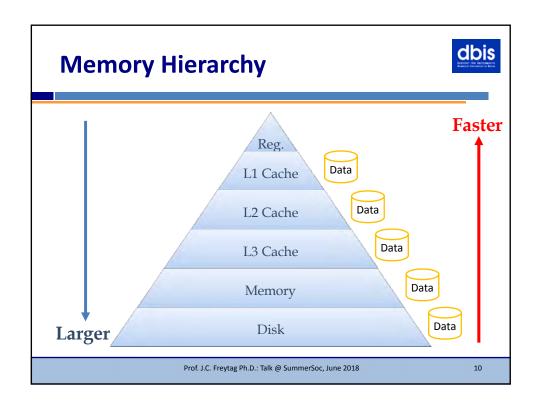
Modern CPUs - Multi-Core & more

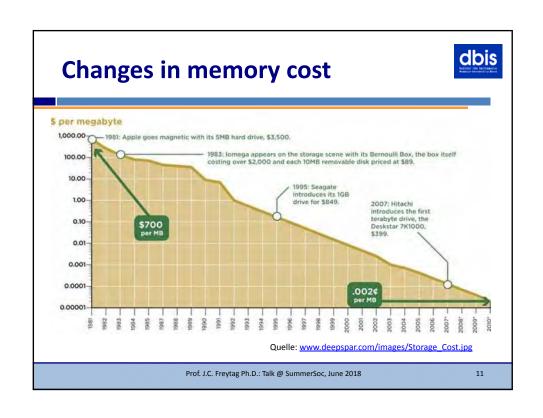


- Features: pipelining, superscalar, branch prediction, prefetching
- Multi-core and simultaneous multi-threading (SMT, hyperthreading)
- SIMD vector instructions (MMX/SSE/AVX)
- Multi-Level cache hierarchy



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Changing technology: Flash disk





- Characteristics
 - Today: 1 TB Cost about \$300 (Samsung)
 - !! Less power consumption !!

Device	Sequential	Random 8KB	Price \$	Power	iops/\$	iops/watt
SCSI 15k rpm	75 MBps	200 iops	500\$	15 watt	0.5	13
SATA 10k rpm	60 MBps	100 iops	150\$	8 watt	0.7	12
Flash- read	53 MBps	2,800 iops	400\$	0.9 watt	7.0	3,100
Flash - write	36 MBps	27 iops	400\$	0.9 watt	0.07	30

Gray, J., & Fitzgerald, B. (2007), FLASH Disk Opportunity for Server-Applications, from http://research.microsoft.com/~Gray/papers/FlashDiskPublic.doc; Jan 2007; Retrieved March 8, 2007

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Changing technology: CPU farms, Clusters & BigData Centers



Compute Container

- > 1200 CPUs
 - > 22000 cores
 - > 5.4 TB Main memory
 - > 7.0 PBytes Disk storage
 - Only Need power & Internet access & water

Big Data Center (Google & others)



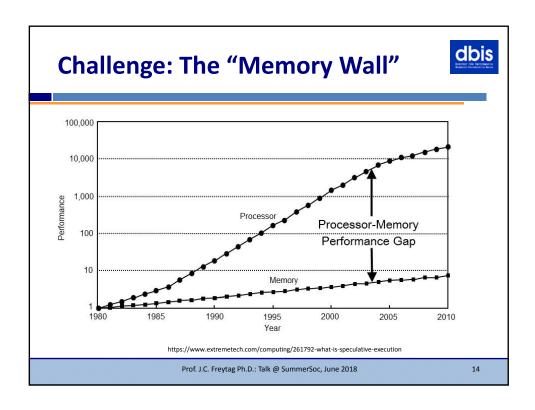




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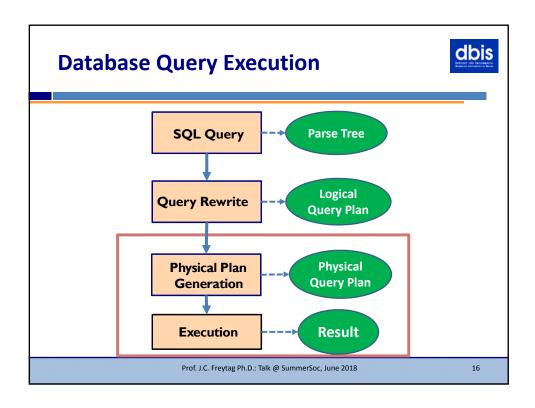


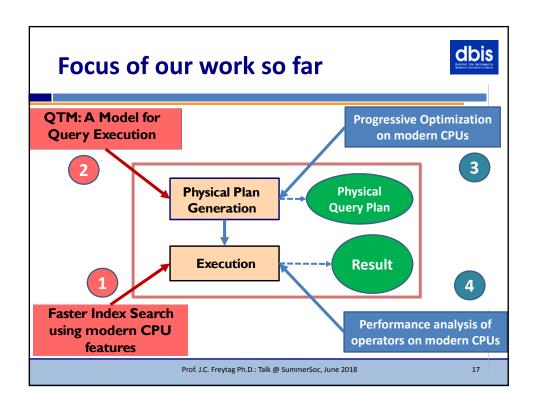
What does it mean for DBMS

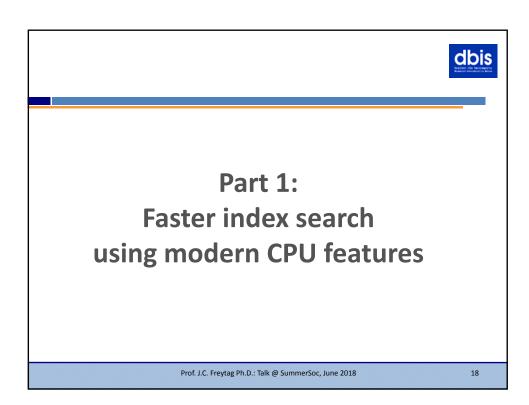


- The world of HW has changed
- The world of data management has changed
 - MapReduce Systems
 - 1st generation: Hadoop, Google proprietary,
 - 2nd generation: Apache Flink (Berlin), Apache Spark (Berkeley)
- Relational DBMS technology has not changed
 - Architecture is 40+ years old
 - Needs rethinking with new HW/OS opportunities
 - Architecture & HW impact
 - From static (2 phase) to dynamic (decide during execution)
 - Include new HW (GPUs, FPGAs, Cluster, ...)

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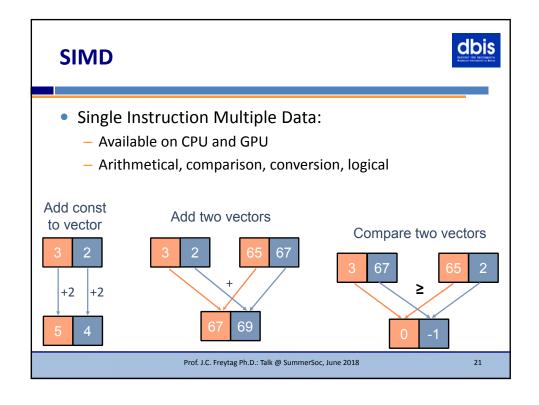


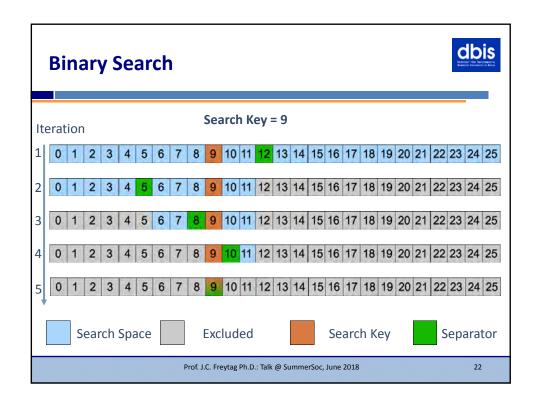


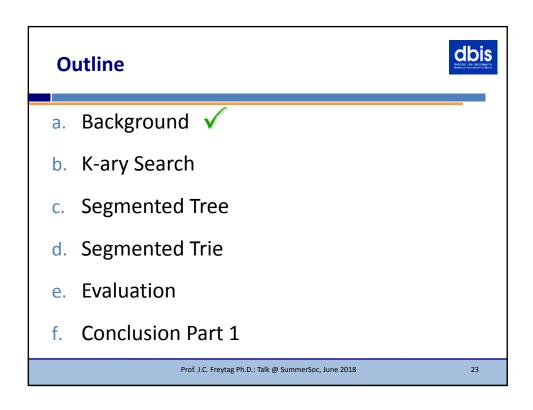


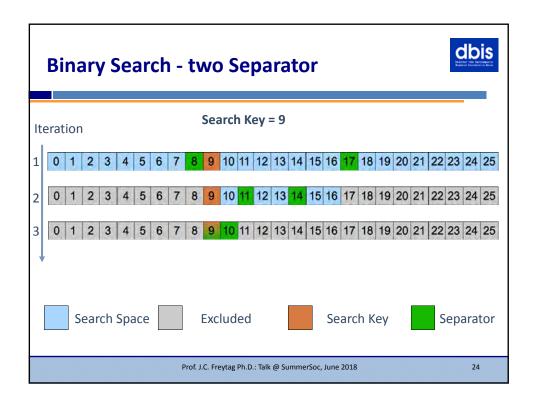
B+-Tree: commonly used index structure Finding a key in O(logbn) Common node-internal search algorithm: Binary search in O(log2n) Can we do better? Yes with SIMD! Prof. J.C. Freytag Ph.D.: Talk @ SummerSoc, June 2018 Prof. J.C. Freytag Ph.D.: Talk @ SummerSoc, June 2018

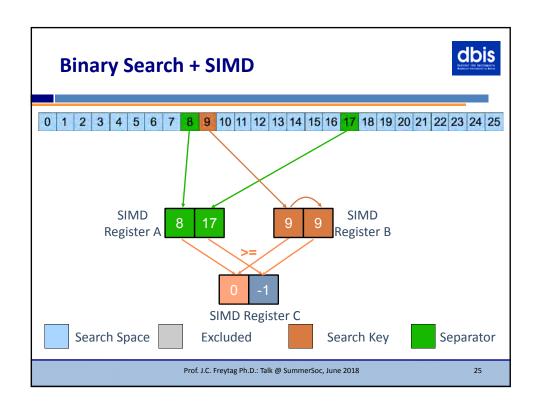
a. Binary Search & SIMD b. K-ary Search c. Segmented Tree d. Segmented Trie e. Evaluation & Contribution

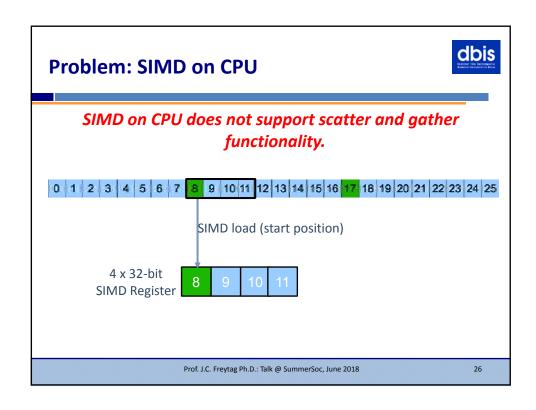


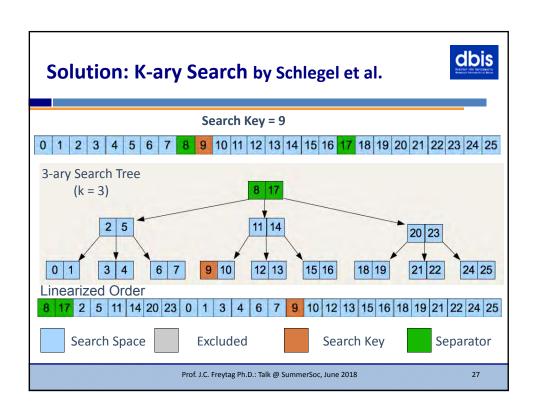


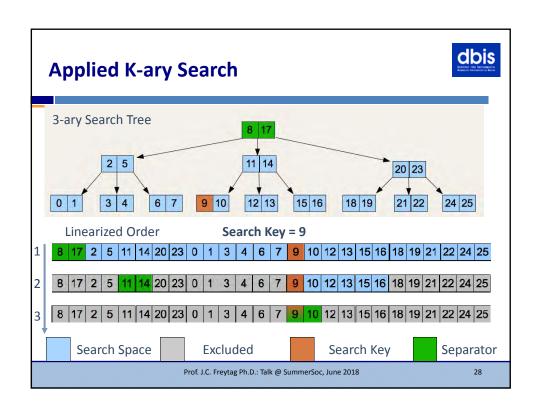


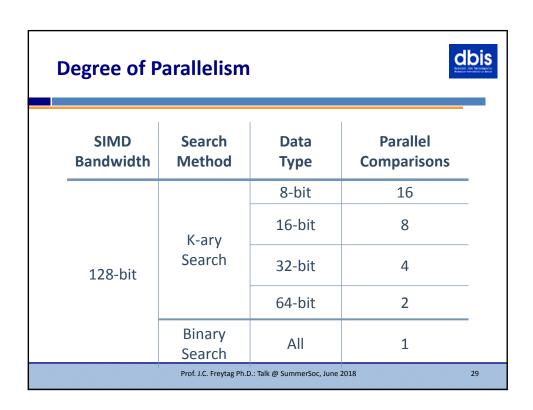




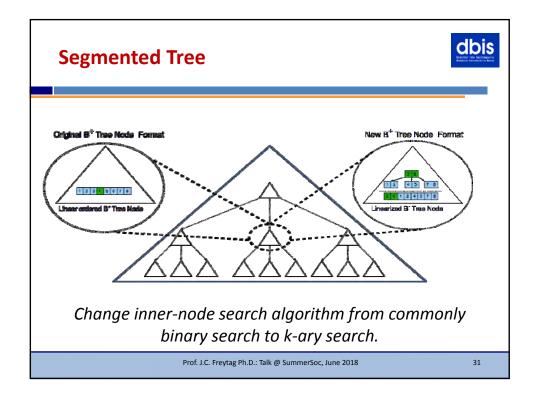


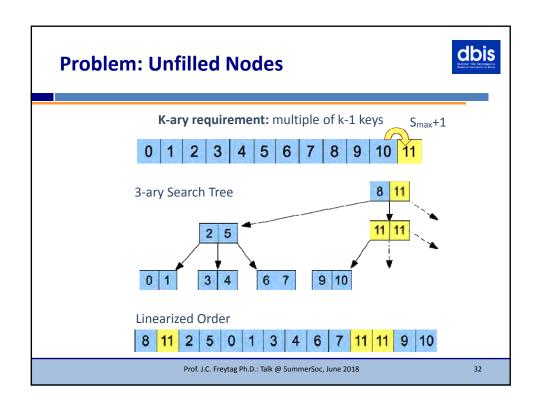






a. Binary Search & SIMD ✓ b. K-ary Search ✓ c. Segmented Tree d. Segmented Trie e. Evaluation f. Conclusion Part 1





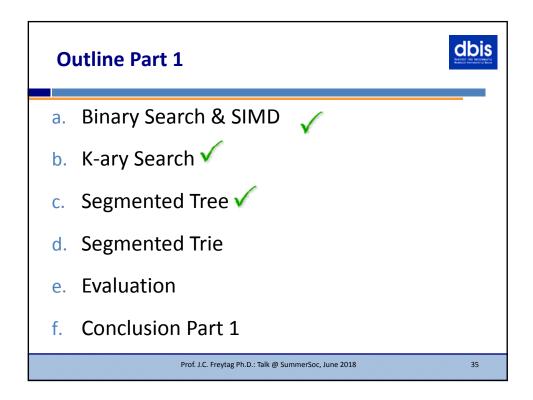
Insert implies Reordering

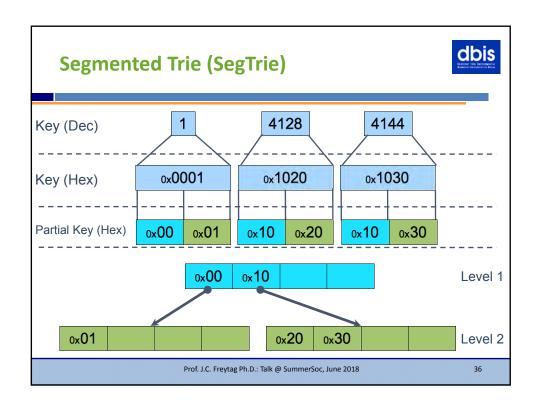


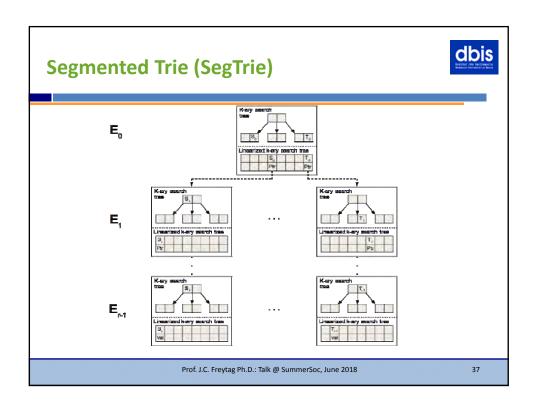
- Inserting a new key requires a reordering if it is inserted between two existing keys:
 - Sorting → Inserting → Linearizing
- Not necessary if:
 - Empty Node
 - Key is greater than the largest existing key

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Advantages: High resource utilization Less iterations required Binary Search: log₂n vs. k-ary Search log_kn Disadvantages: Reordering overhead Large data types decrease performance Open/Challenge: Updates







Segmented Trie (SegTrie)



Advantages:

- High SIMD search performance
- Prefix compression
- Early termination

Disadvantages:

- Fix level count
- Reordering overhead

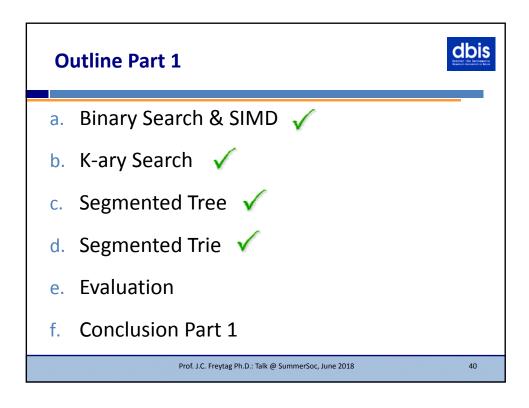
Upen/Challenge:

Updates

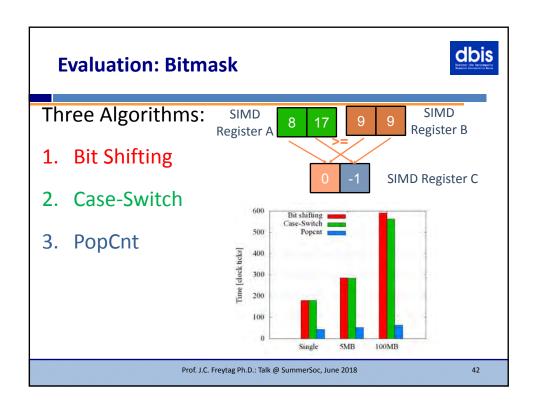
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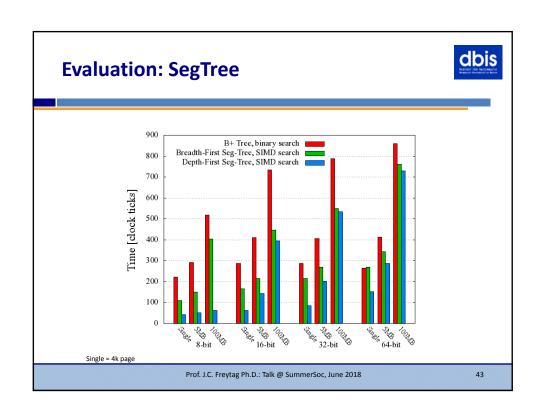
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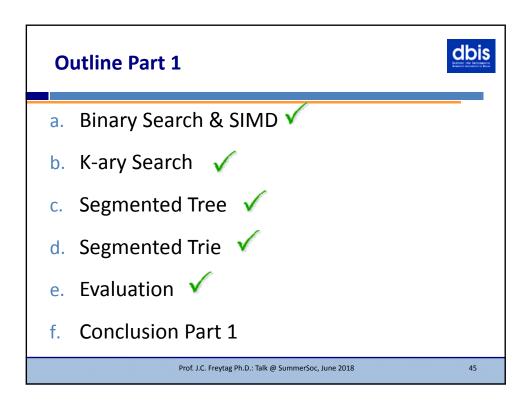
dbis SegmentedTree vs. Segmented Trie SegTree SegTrie Derived **Prefix** B+-Tree **B-Tree** From Number of Max. #Level Tree Height **Iterations** (Early termination) Number of Dynamic Static (Pre-defined) Level DOP Depends on 16 (8-bit) Data Type Prof. J.C. Freytag Ph.D.: Talk @ SummerSoc, June 2018



Test Setup HW/SW Configuration: CPU: Intel Xeon 5520, 4 x 2,26 GHz L1: 32KB, L2: 256 KB, L3: 8 MB, MM: 8 GB Cacheline: 128 Byte, SIMD bandwidth: 128 Bit Windows 7 64-bit Professional Test Dataset: Synthetically generated, ascending, starting at 0





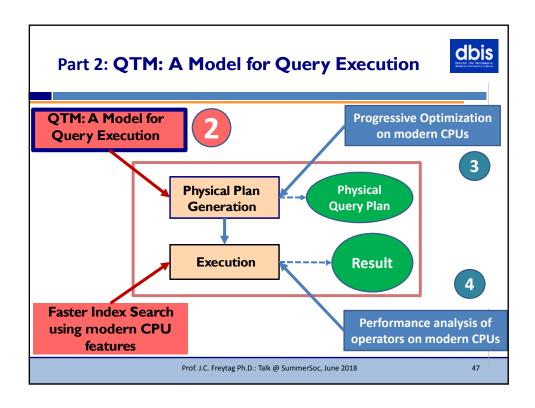


Using SIMD B+-Tree -> Segmented Tree Prefix B-Tree -> Segmented Trie Transformation and search algorithm using breadth-first and depth-first data layout Three algorithms for interpreting SIMD comparison results

Our Contributions - Part 1

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Generalization for an arbitrary key count ("Filling up")



Motivation



- Different DBMS execute the same QEP using different schedules
 - Run-time execution not query optimization
 - No uniform scheduling format
 - Query execution in different DBMS are not comparable
- Major differences between DBMS:
 - Chunk Size: Size of operator's input
 - Scheduling Strategy: Execution model vs. run-time scheduler

How to make different schedules comparable to explain why one schedule performs better than another?

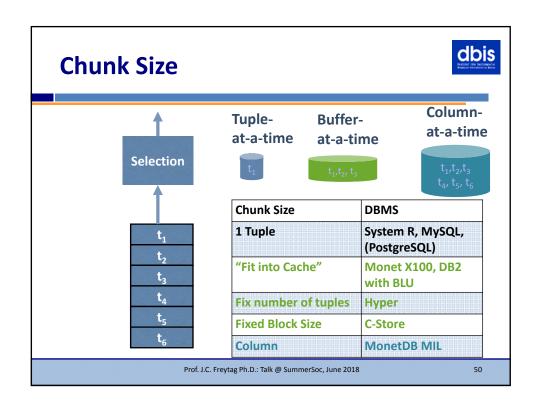
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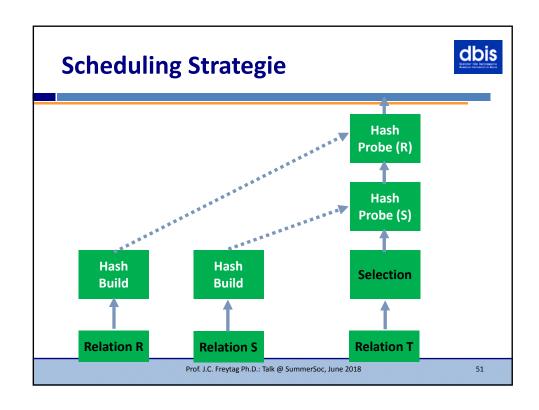
Outline Part 2

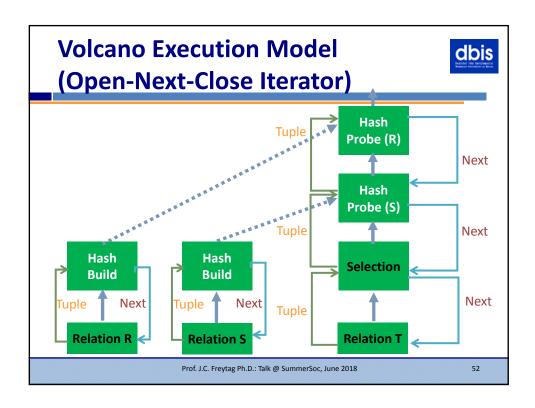


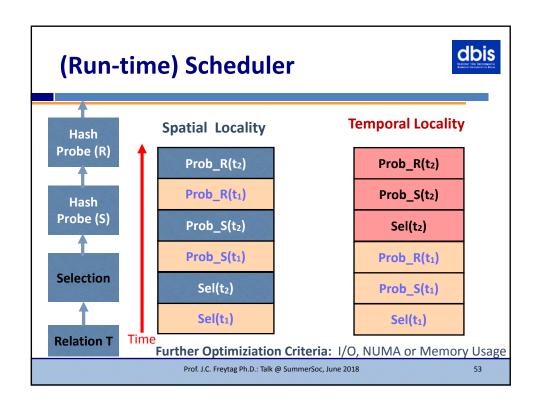
- a. Parallel Query Execution
- b. QTM: Query Task Model
- c. Evaluation
- d. Outlook

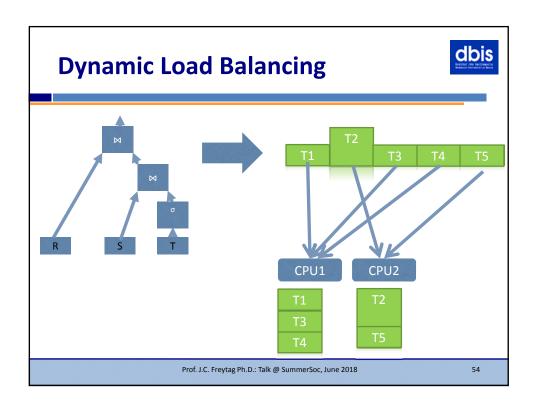
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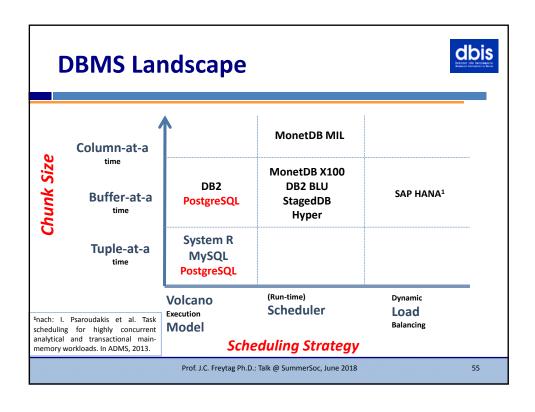


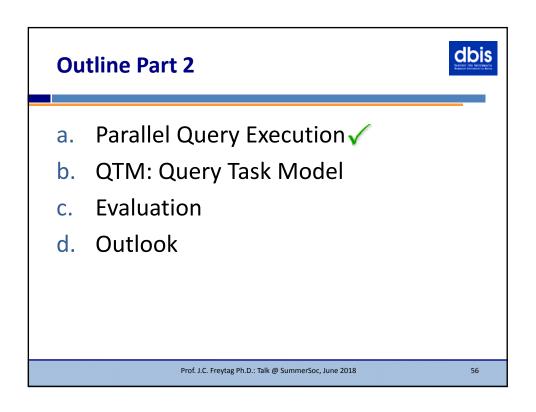










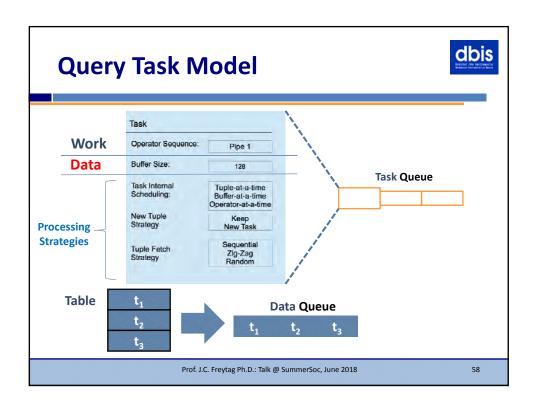


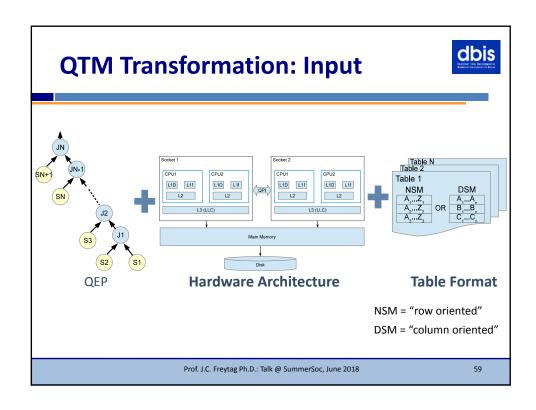
QTM: Query Task Model

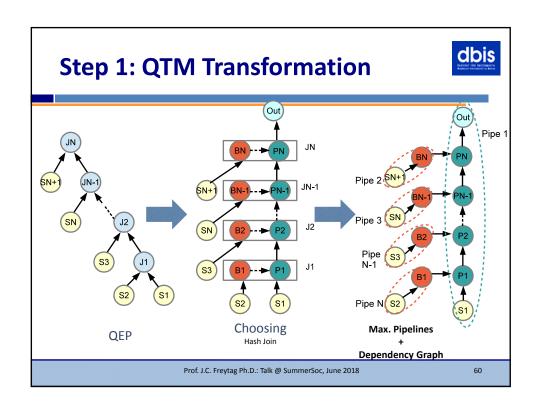


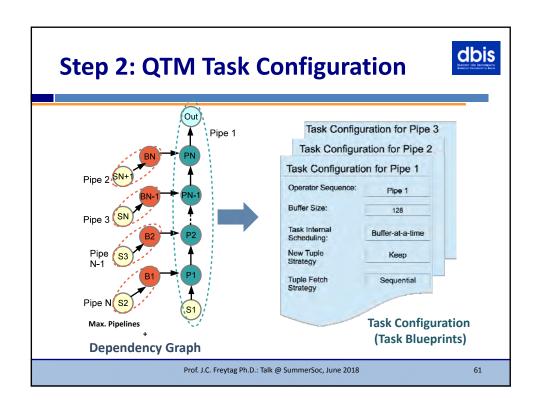
- Idea: A model that describes parallel query execution with tasks
 - QEP → Queue of tasks
 - Task: Encapsulates a <u>piece of work on some data</u>
- Goal:
 - Open a design space for DBMS schedules
 - Make main aspects of query scheduling comparable:
 Execution order, degree of parallelism and thread coordination, and partitioning

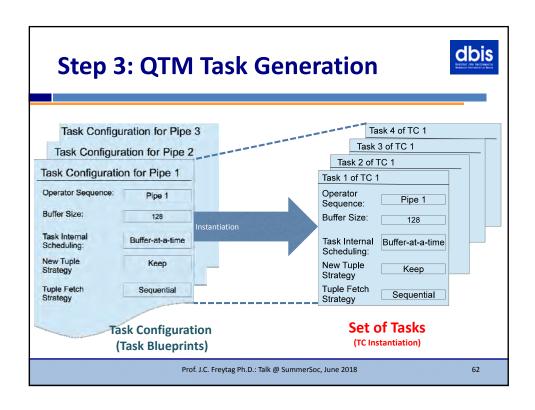
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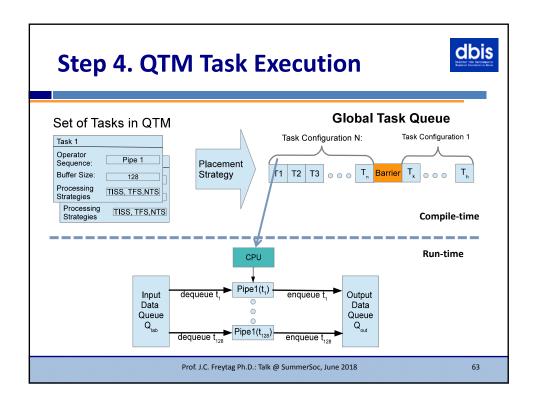


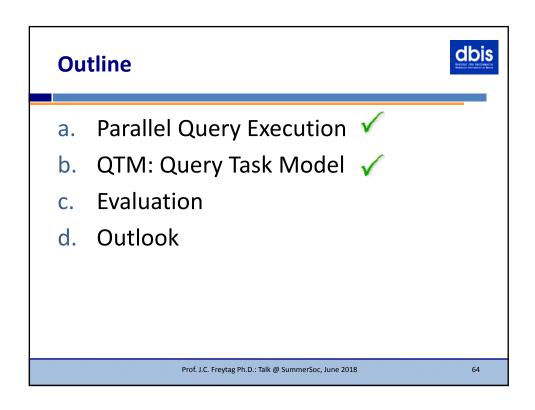


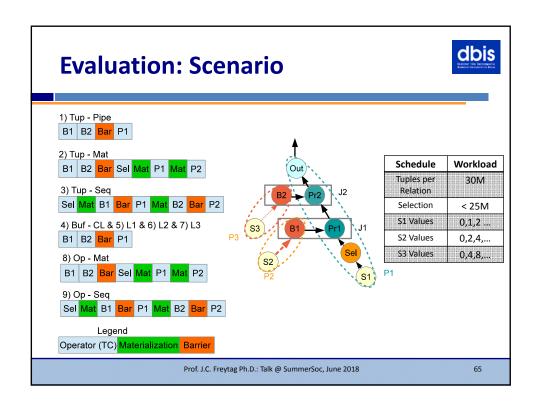


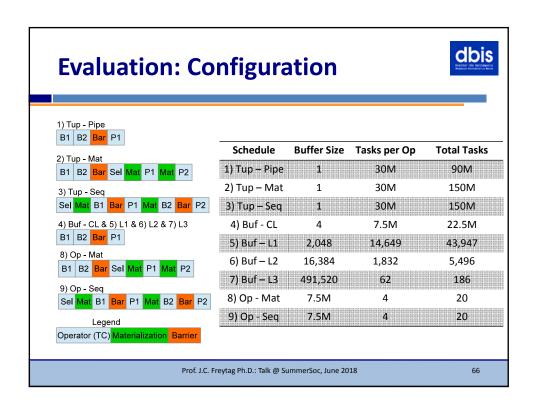


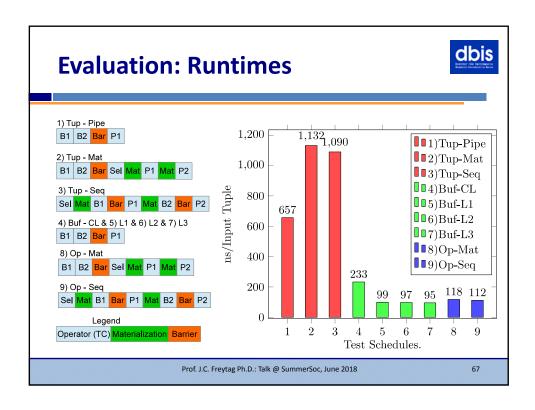










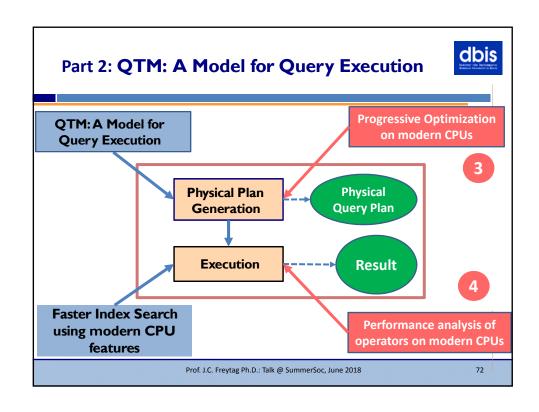


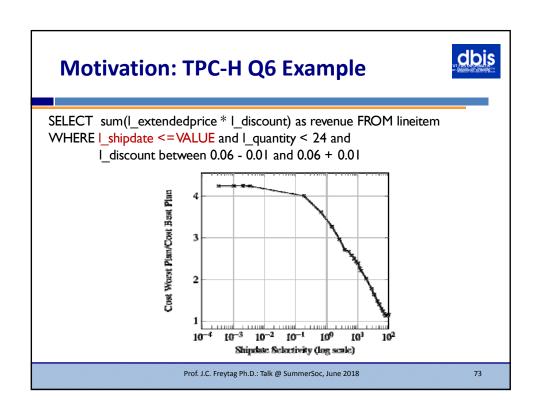
Evaluation: Insights



- Tradeoff between data and instruction cache performance
- Medium sized tasks are data-efficient:
 - Pros: Buffer fits entirely into cache, high data locality
 - Cons: High number of tasks and instructions
- Large tasks are instruction-efficient:
 - Pros: Decrease number of instructions and tasks, high instruction locality
 - Cons: More data cache misses if cache size is exceeded

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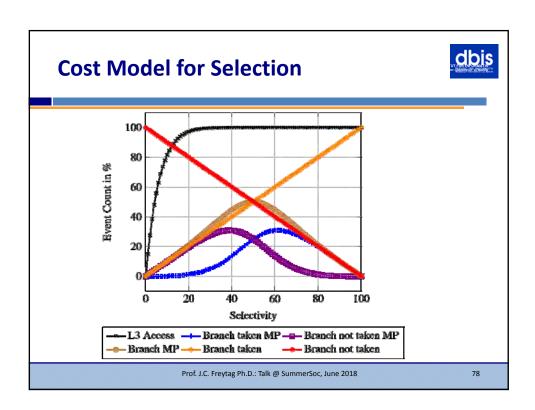


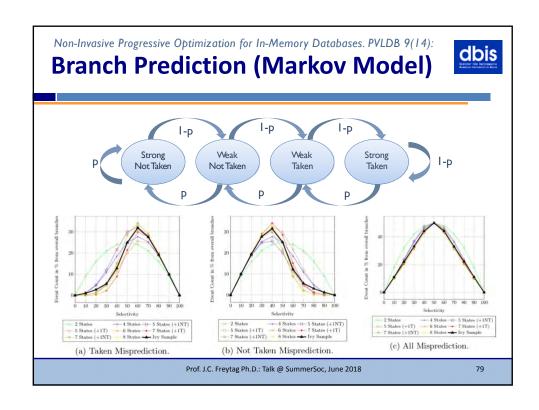
Approach: Steps Taken (Selections)

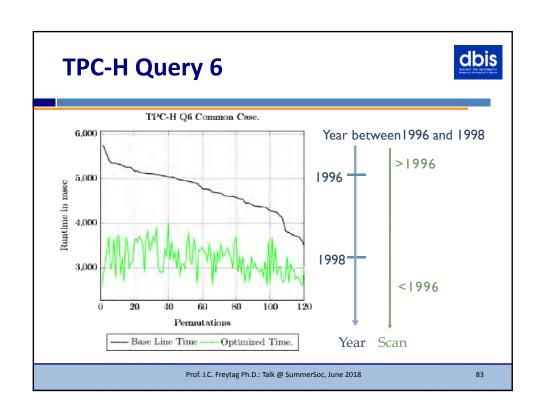


- Use CPU counters
- 2. Thorough analysis (understanding) of operators with respect to CPU counters
- 3. From data to knowledge:
 - Interpret counters in the context of selections
- 4. Build model
 - Compare actual counters vs. predicted (by model)
 - Validate model extensively
- 5. Optimization algorithm by continuous observation (actual) and adjustment (predicted vs. actual)

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Contribution



- Markov model for branch prediction
- From Data to Knowledge: Interpreting counters for need to optimize
- Algorithm for continuous optimization of a sequence of selections
- Future: extend approach for joins (partially addressed in paper)

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Publications



- QTM: Modelling Query Execution with Tasks, ADMS 2014
- Adapting Tree Structures for Processing with SIMD Instructions, EDBT 2014
- Selection on Modern CPUs, IMDM 2015
- Non-Invasive Progressive Optimization for In-Memory Databases, PVLDB 9(14) 2016

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