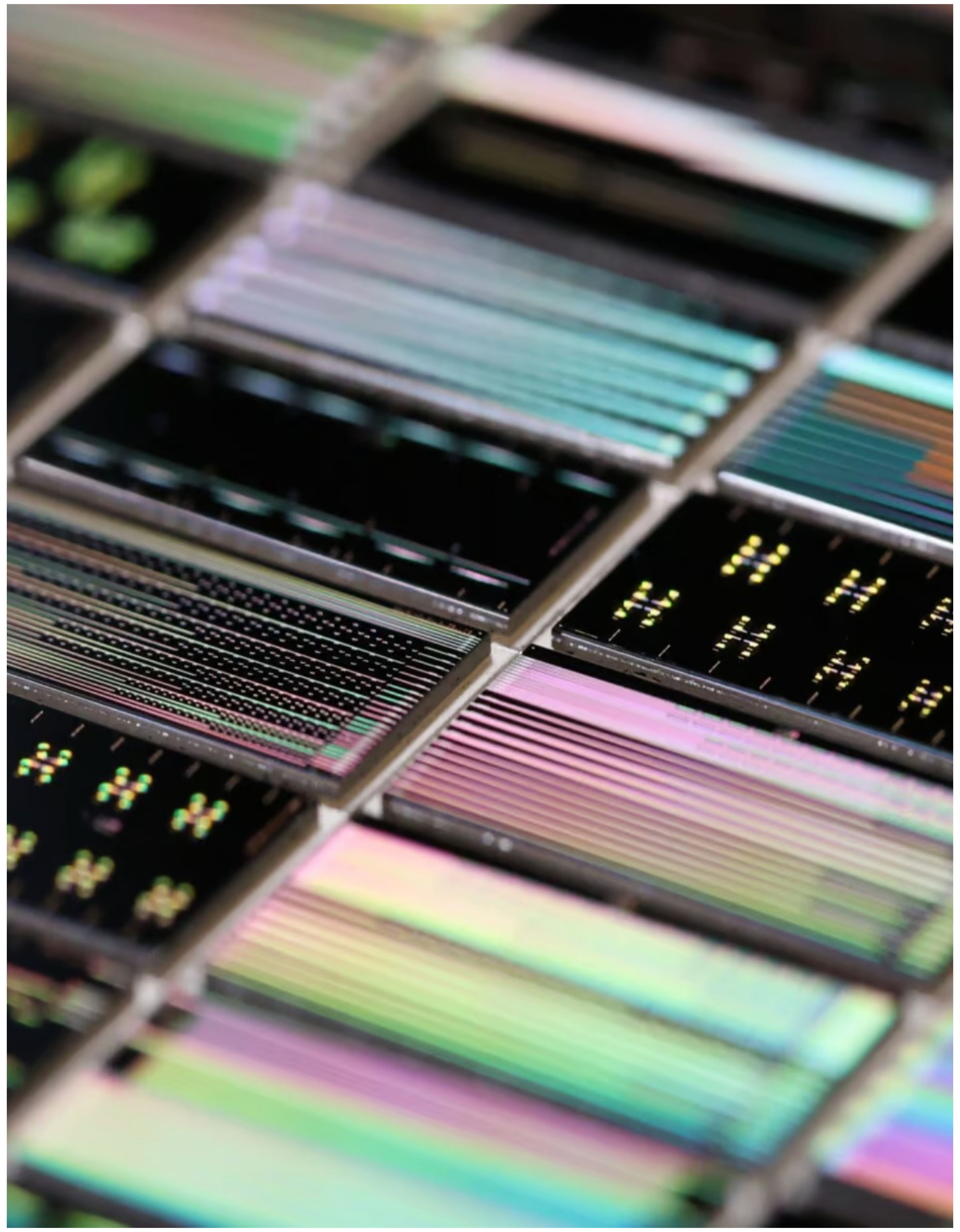
Photonic Quantum Technologies



Dr. Michael Förtsch
Founder & CEO
24. June 2024
Prepared for SOC Summer School 2024

Q.ANT

Q.ANT

Short Introduction

Fast development and prototyping led us to 3 World Premiers
made possible by a strong expert team, partner landscape and IP portfolio.

2018
Foundation

4
Product Lines

2.300
sqm Workspace

100+
Q.ANTies

17
Nationalities

6
Publicly funded projects

51
Patent Families

3
World Premiers [1,2]

7
Coffee machines[3]

[1] www.produktion.de/technik/zukunftstechnologien/quantentechnologie/erste-industriefaehige-quantensensoren-sind-im-einsatz-44-344.html
[2] qant.com/press-releases/q-ant-presents-the-potentials-of-quantum-technology-at-the-hannover-fair/
[3] Our fast pace took toll on 7 coffee machines thus far ;)

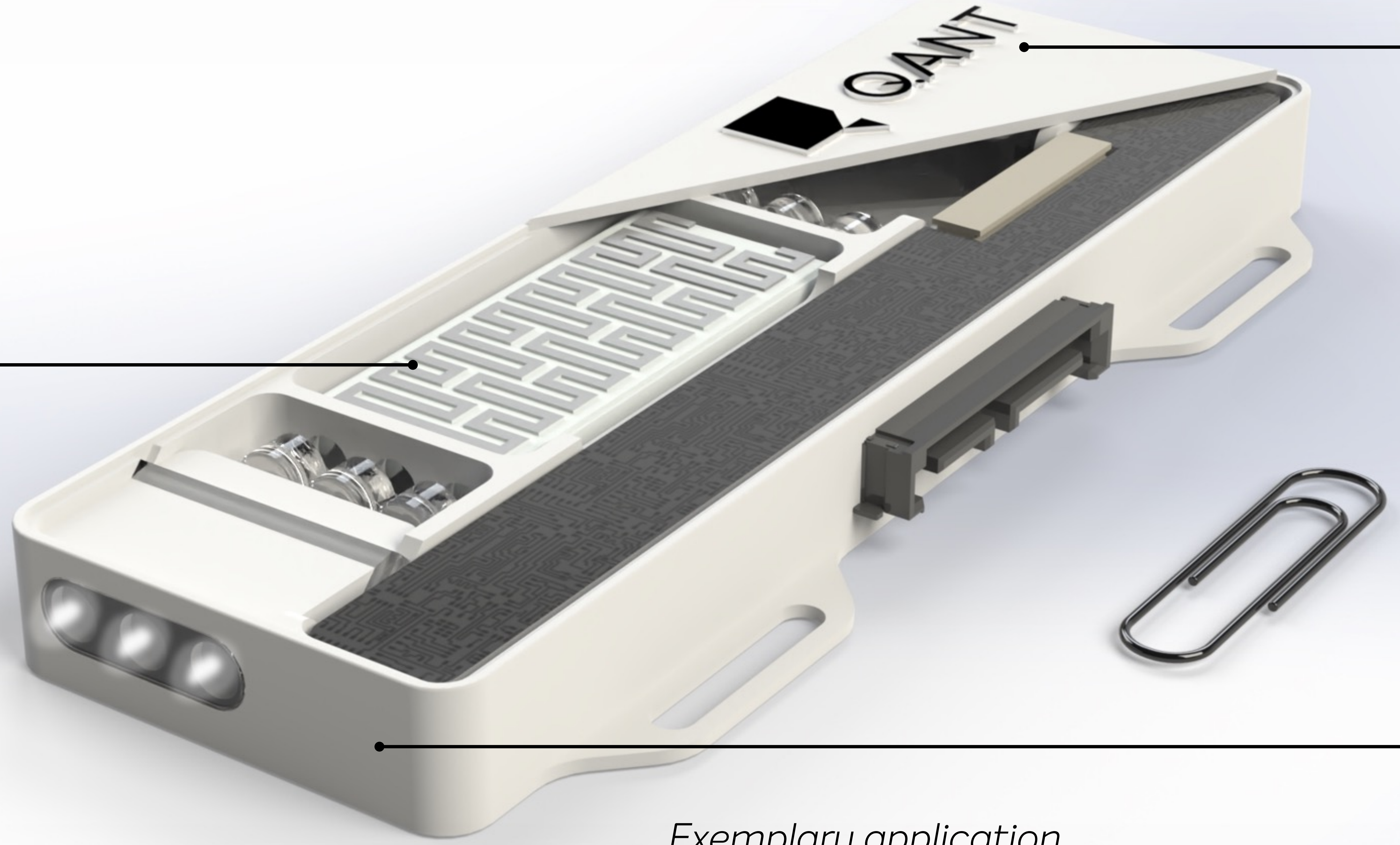
Q.ANT backbone is its Photonic Framework Para.Digm …

… realizes the next level of data generation and data processing.

Q.ANT inside

Quantum controls

- Nonlinear waveguides
- Tailored optical elements



Exemplary application

Electron to photon conversion

- Solid state diodes
- Low-noise current drivers

Photon to Electron conversion

- Low-noise amplifiers
- Analog to Digital conversion
- Signal process

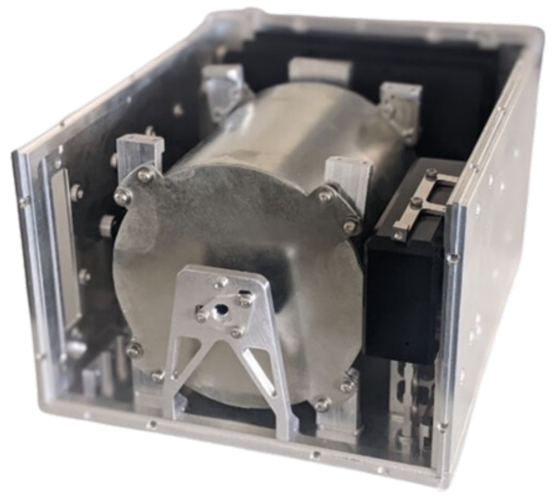
Q.ANT realizes the next level of data generation and data processing
in the following four product lines

Data generation

Particle Metrology

Sensor for analyzing finest particles in gases, liquids and as powders.

Atomic Gyroscope



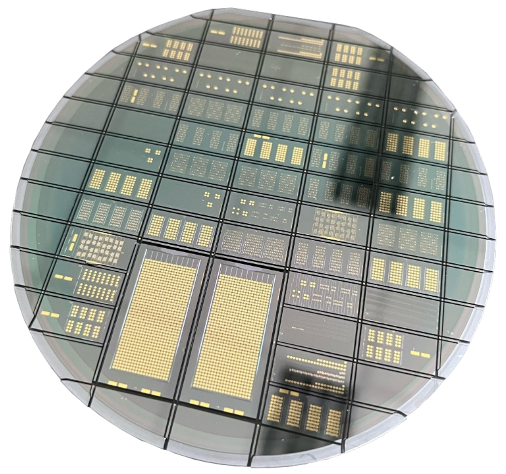
Sensor for stabilization and localization of systems.

Magnetic Sensing

Sensor for measuring electrical bio signals

Data processing

Photonic Computing



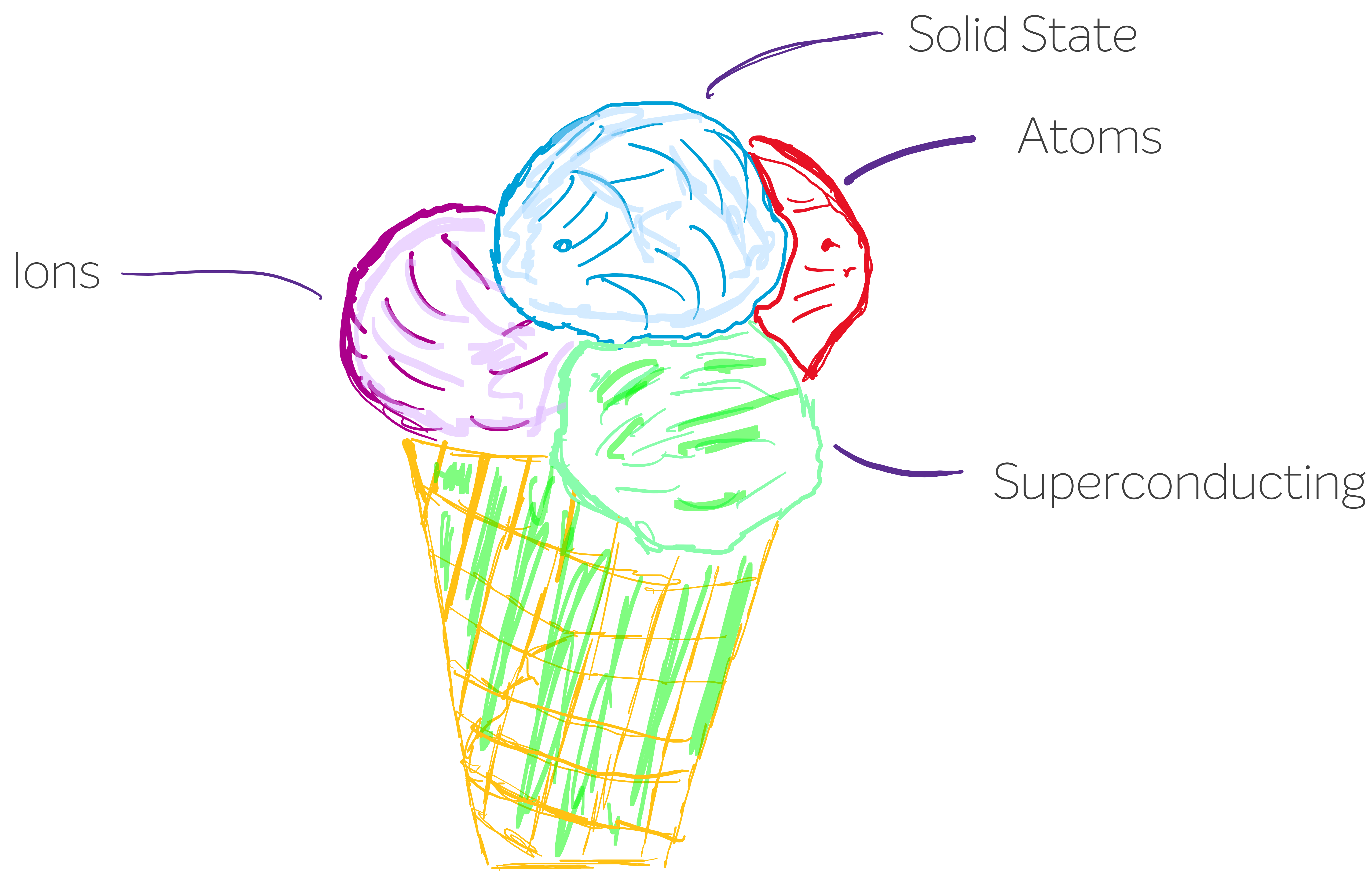
Photonic chips and computing for solving complex algorithms.

Our new magnetic field sensor was a big attraction on the Hannover fair 2024
with a live detection of muscle signals, bringing humans and machines closer.

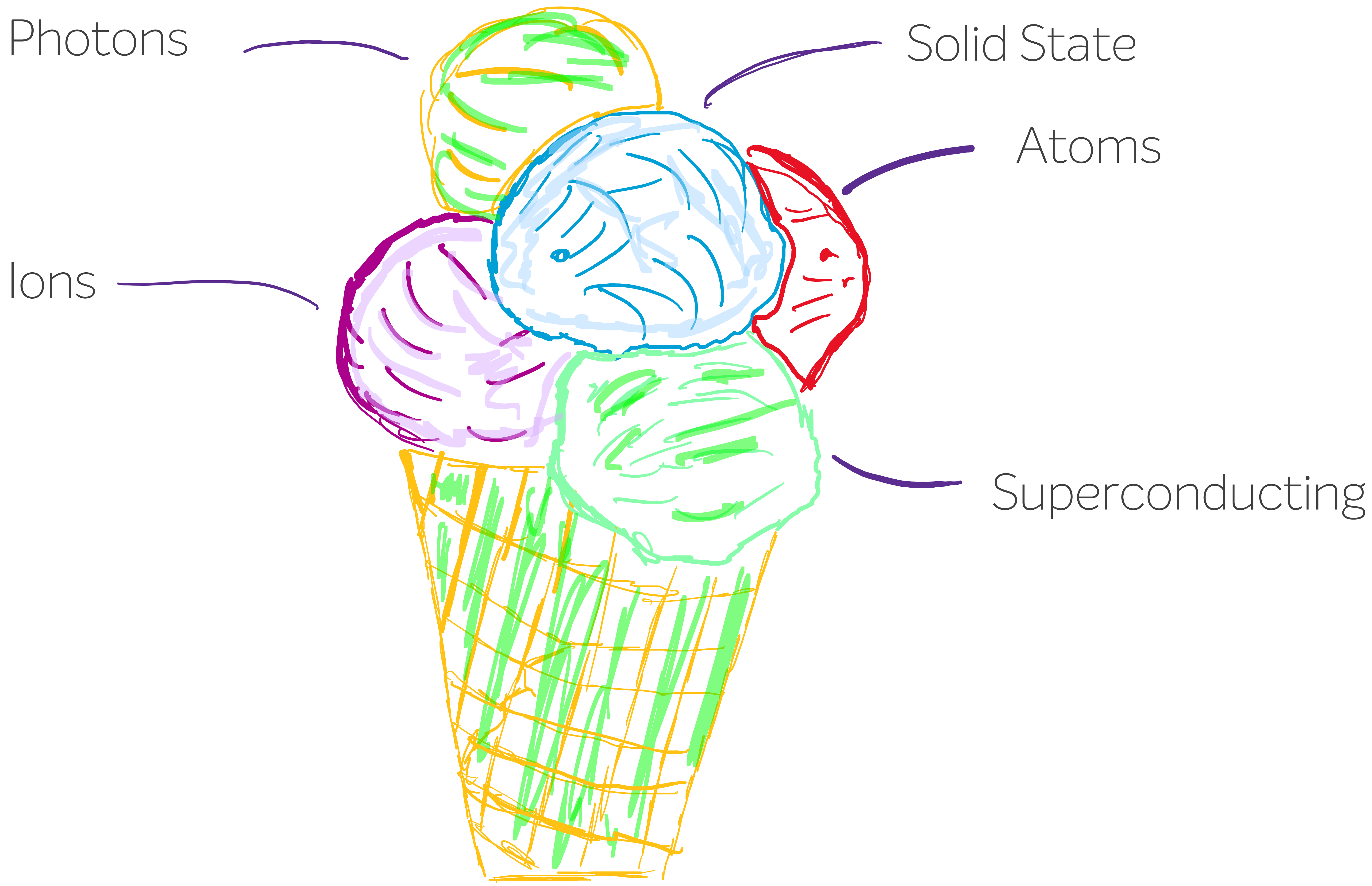
Photonic Computing

For Classic and Quantum

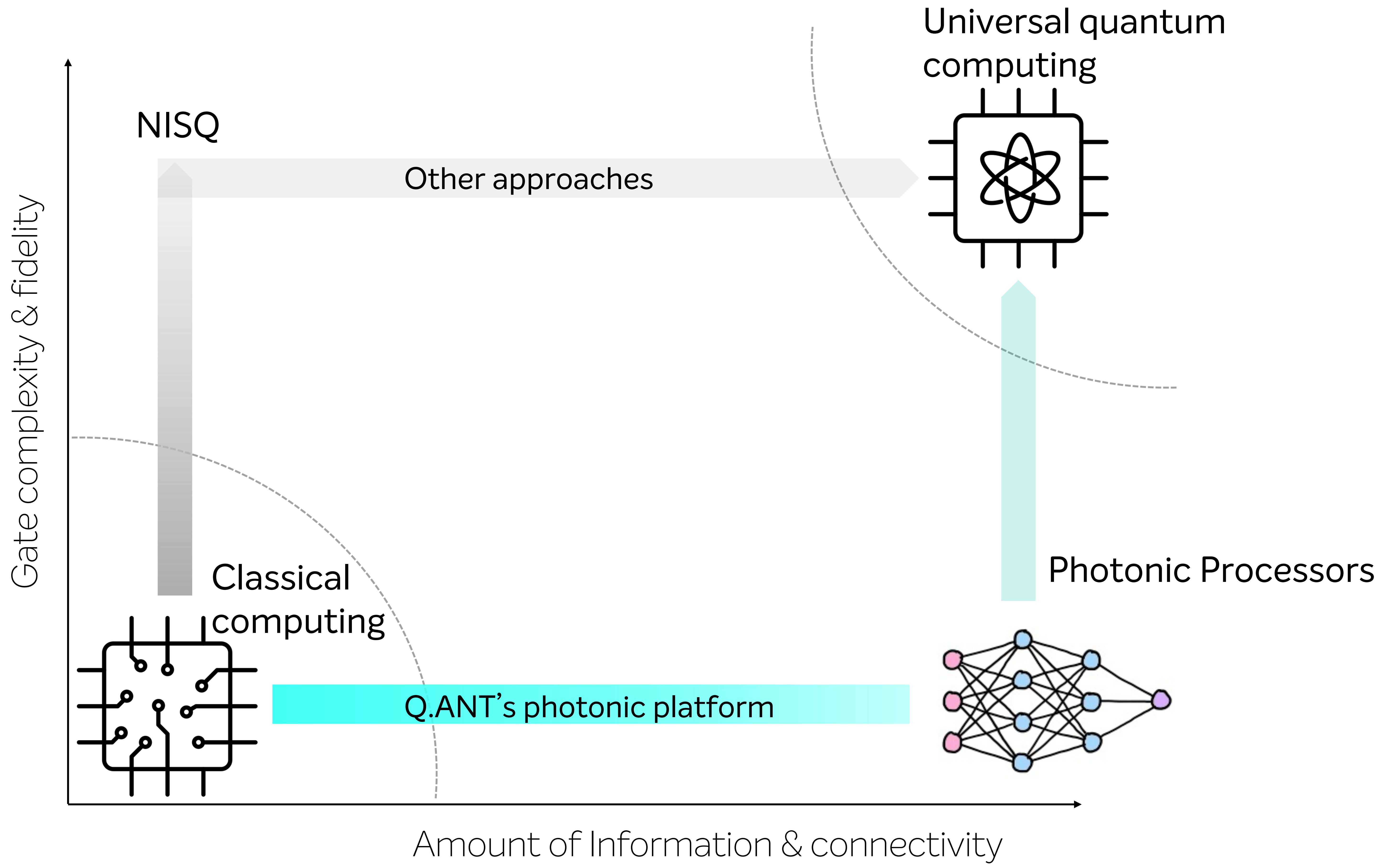
Many approaches are racing towards a productive Quantum Computer.



Do we need an additional platform based on Photons?



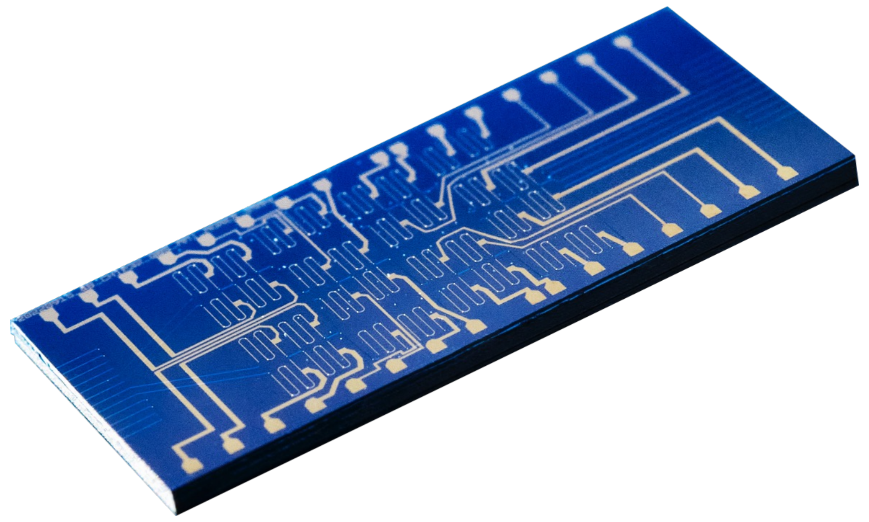
Photonic Computing is a novel approach to the next level of computing.



One technology – multiple applications for data processing

Photonic integrated chips open up a wide range of applications.

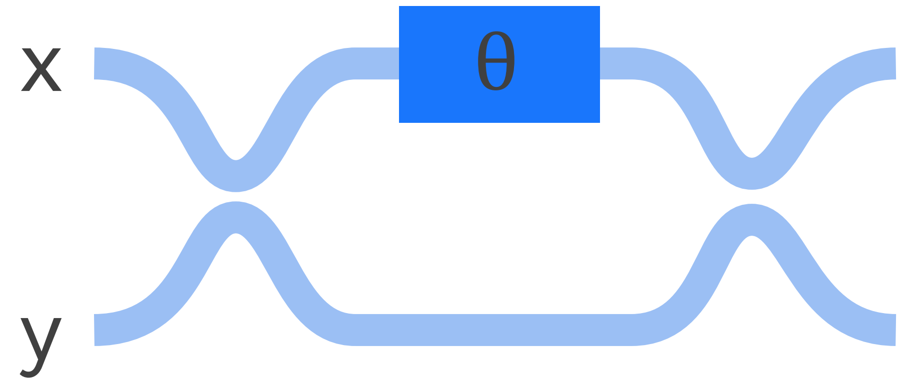
Algorithm	Abstraction	Photonic Chip
AI acceleration Optimization via Ising Machine Neuromorphic computing	Classical Analog computing	
Chemistry simulation Material Simulation	Quantum Computing	



Analog computing

Photons natively implement addition/subtraction as well as multiplication

Variable beamsplitters natively add and subtract the two inputs in parallel

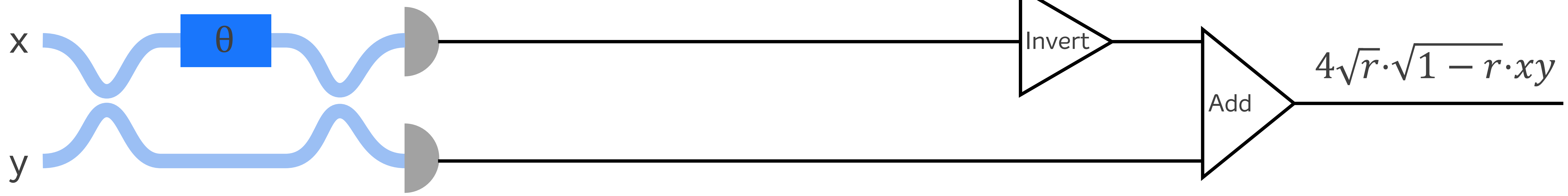


$\sqrt{r}\cdot x - \sqrt{1-r}\cdot y$

$\sqrt{r}\cdot x + \sqrt{1-r}\cdot y$

Detectors natively square the inputs, implementing several multiplications in parallel

$(\sqrt{r}\cdot x - \sqrt{1-r}\cdot y)^2 =$
$r\cdot x^2 - 2\sqrt{r}\sqrt{1-r}\cdot xy + (1-r)\cdot y^2$

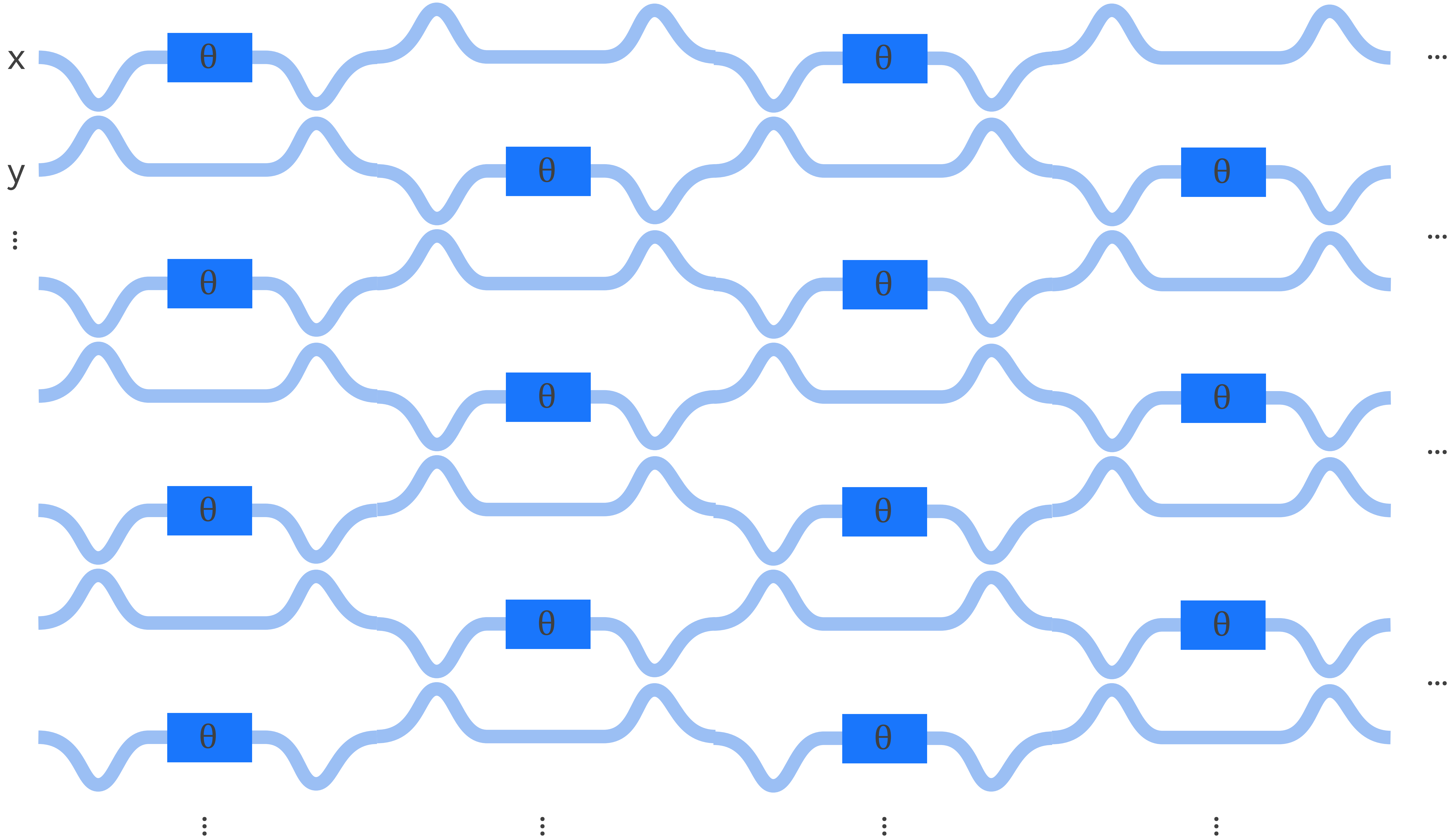


$4\sqrt{r}\cdot\sqrt{1-r}\cdot xy$

$(\sqrt{r}\cdot x + \sqrt{1-r}\cdot y)^2 =$
$r\cdot x^2 + 2\sqrt{r}\sqrt{1-r}\cdot xy + (1-r)\cdot y^2$

We can scale this up thanks to our photonic integrated circuit platform

to reach even higher levels on parallelism



Q.ANT

On a fundamental level, all applications require two features:

high nonlinearity combined and fast matrix multiplication.

Chip Features

High Nonlinearity

Fast Matrix Multiplier

Q.ANT LNOI photonic integrated chips technology

Chip Architecture

Gaussian Boson Sampling	Multiphoton states	+	Multipath interference	+	Single-photon detection
AI Accelerator for Neuronal Networks	Matrix multiplication	+	Non-linear activation function		
Coherent Ising Machine	Nonlinear competition	+	Mixing	+	Feedback loop

Q.ANT's chip architecture is based on Lithium Niobate on Insulator (LNOI)

which combines both features: high nonlinearities with matrix multiplication.

Chip Features

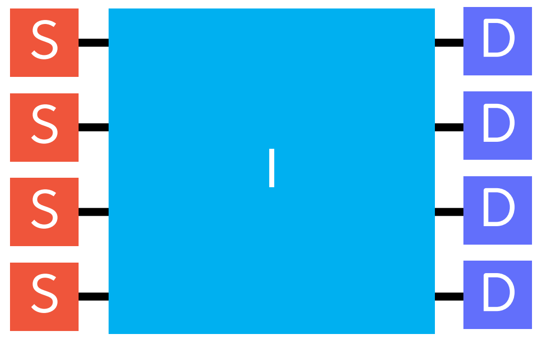
High Nonlinearity

Fast Matrix Multiplier

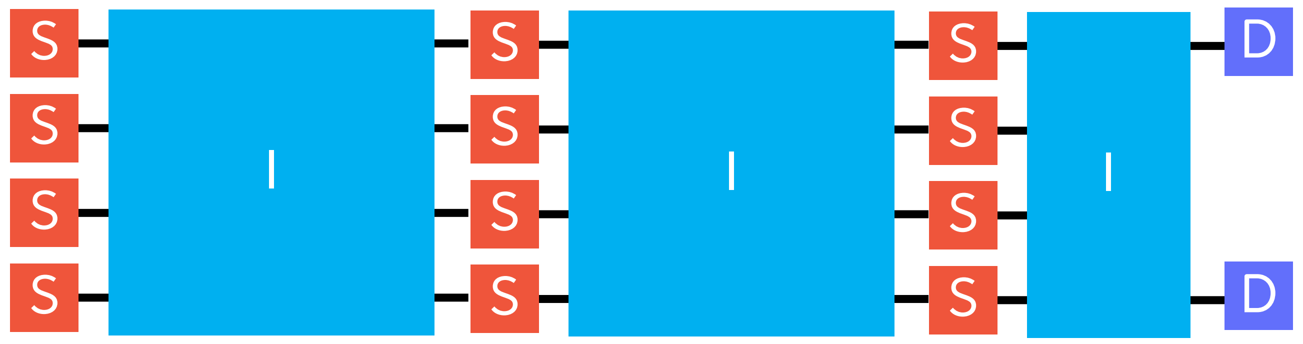
Q.ANT LNOI photonic integrated chips technology

Chip Architecture

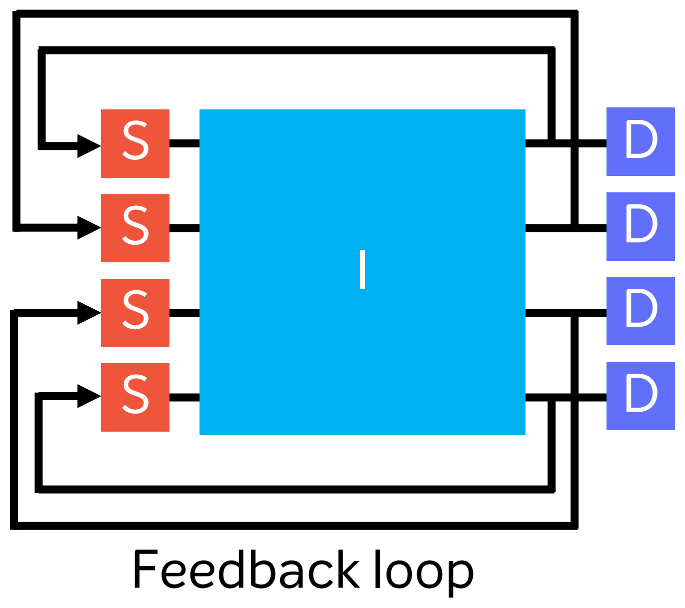
Gaussian Boson Sampling



AI Accelerator for Neuronal Networks



Coherent Ising Machine



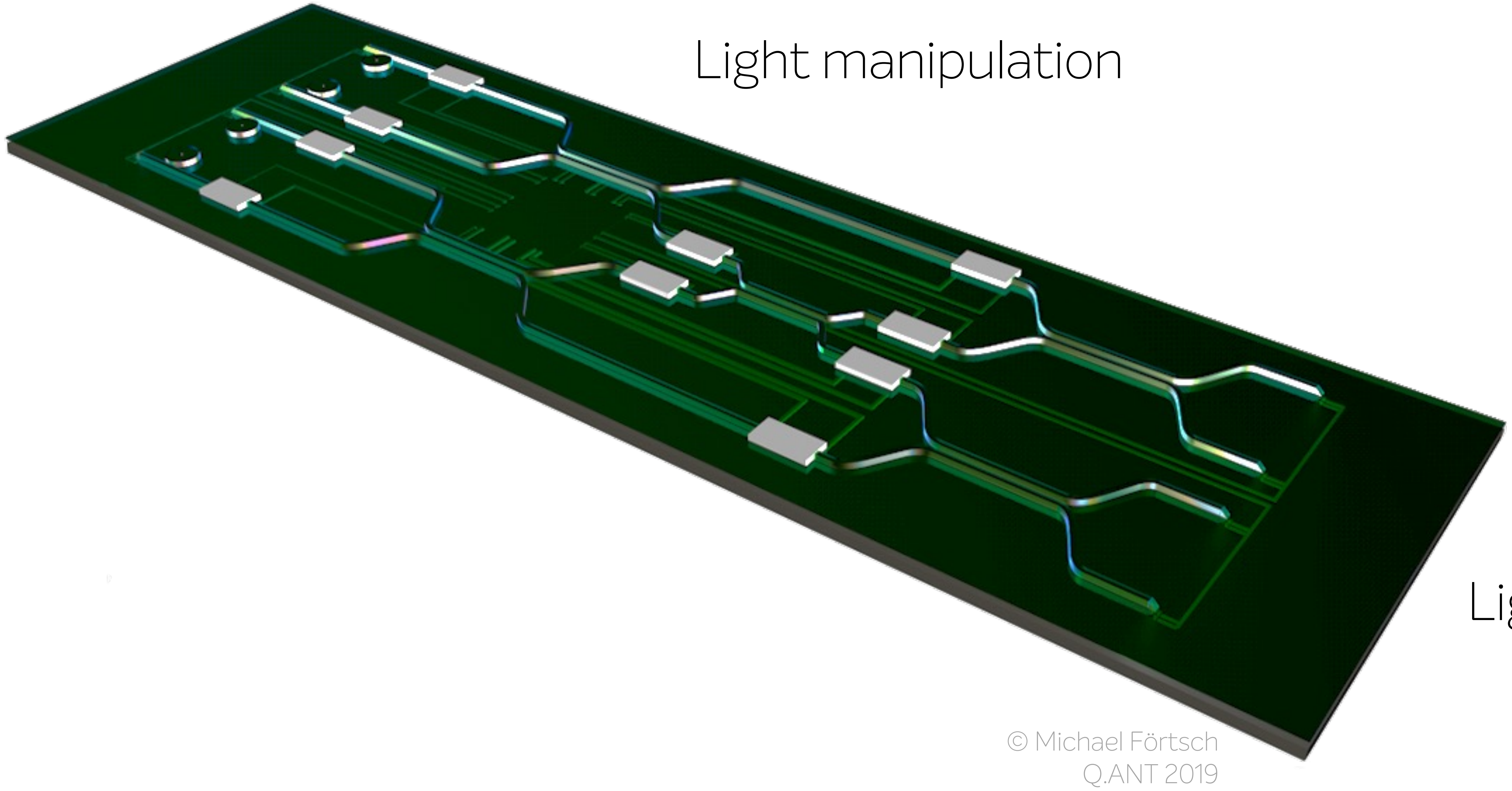
S Squeezer (nonlinearity)
I Interferometer (matrix mult.)
D Detector

Q.ANT's chip architecture is based on Lithium Niobate on Insulator (LNOI)

which combines both features: high nonlinearities with matrix multiplication.

Light generation

Light manipulation



Light detection

Q.ANT

There is no photonic silicon – Multiple materials compete in integrated photonics.

LNOI/ TFLN has advantageous properties but is not standard Fab compatible.

	InP/ InGaAs	AlGaAs/ GaAs	Silicon/Ge	SiN	Polymers	Glass / Silica	LNOI / TFLN
Passive components	+	+	++	+++	+++	+++	+++ 👍
Polarization components	++	+	+	++	+	Hybrid	+++ 👍
Lasers	+++	++	Hybrid	Hybrid	Hybrid	Hybrid	Hybrid
Modulators	+++	Hybrid	+	Thermal	++	Hybrid / Thermal	+++ 👍
Switches	++	+	+	+	+	+	+++ 👍
Optical amplifiers	+++	+++	Hybrid	Hybrid	Hybrid	Hybrid	Hybrid
Detectors	+++	+++	++	Hybrid	Hybrid	Hybrid	Hybrid
Losses (dB/cm)	2	2	2	0.1	1.0	0.5	0.1 👍
2. order non-linearity	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	+++ 👍
Wafer-size	4"	3-6"	6-12"	6-12"	> 8"	6-12"	3-6"
Supply Chain	critical	critical	uncritical	uncritical	uncritical	uncritical	critical
PROs	Best for laser integration	Best for laser integration	CMOS compatible	Low cost Small size	Compatible with Si/InP platforms	Low cost	Very good modulation
CONs	High cost and low yield for components integrating other elements	High cost and low yield for components integrating other elements	No good optical material	Slow Modulators Material properties are process-dependent	Reliability/thermal management issues	No active functionalities	Not standard Fab compatible

Source: Yole report; Expert interviews

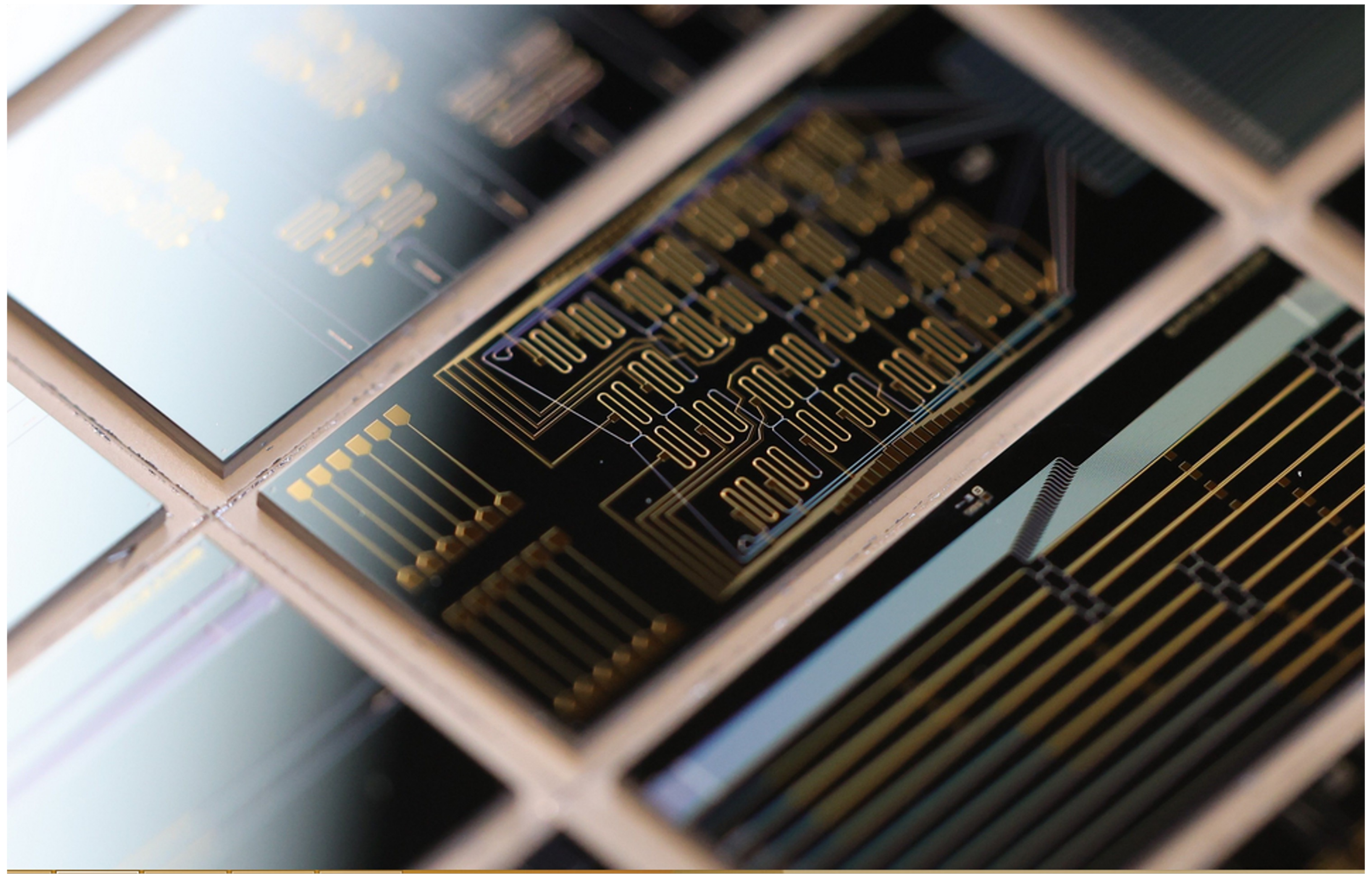
\+ Moderate performance ++ Good performance +++ Strong performance Hybrid Ability in combination with other PIC

Status June 2023: First 4 x 4 matrix chip realized, 20 x 20 in layout

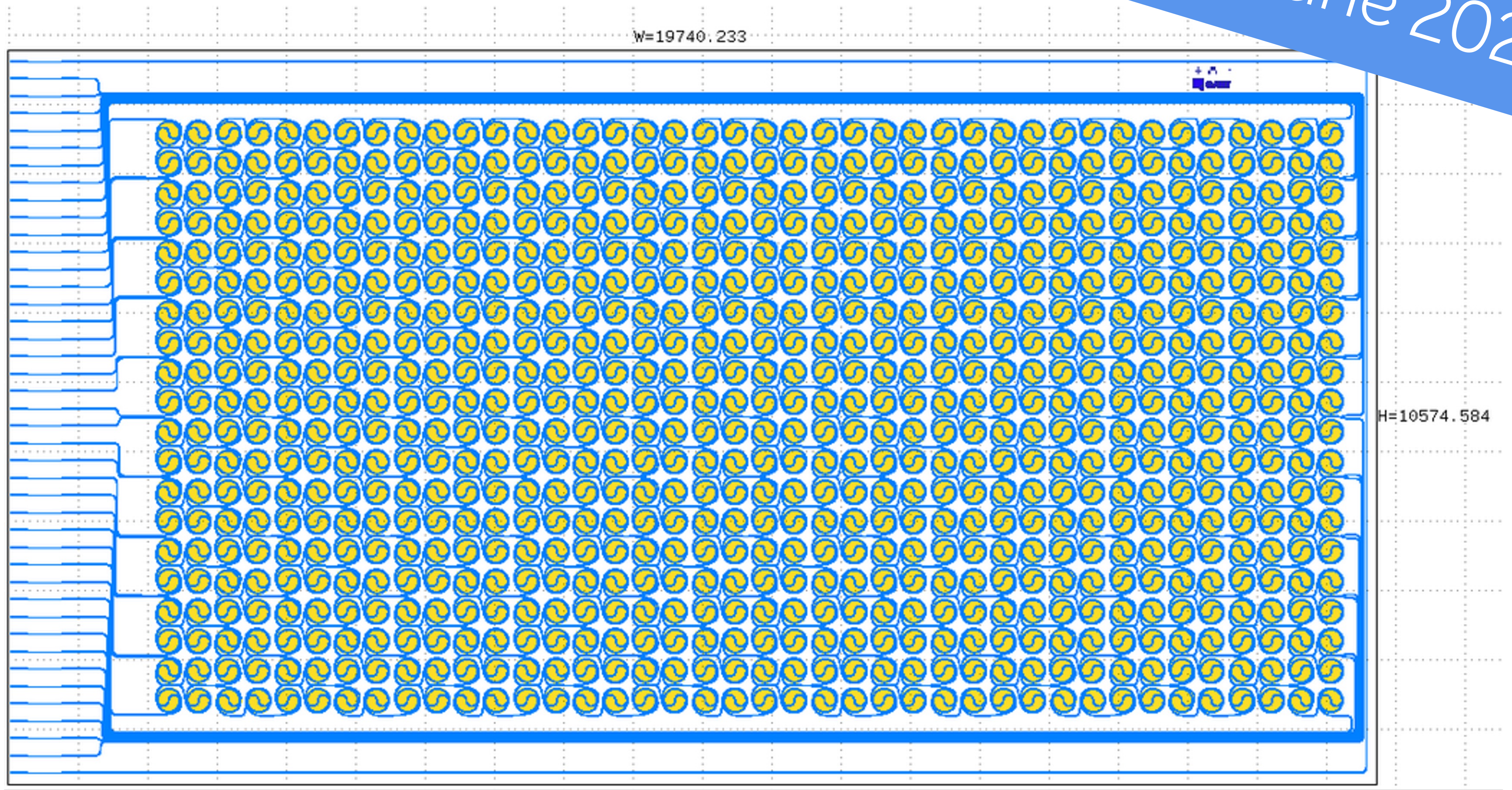
Fabrication status: 4 x 4 photonic integrated chip

Status June 2023

Fabrication status: 4 x 4 photonic integrated chip



Layout status: 20 x 20 chip



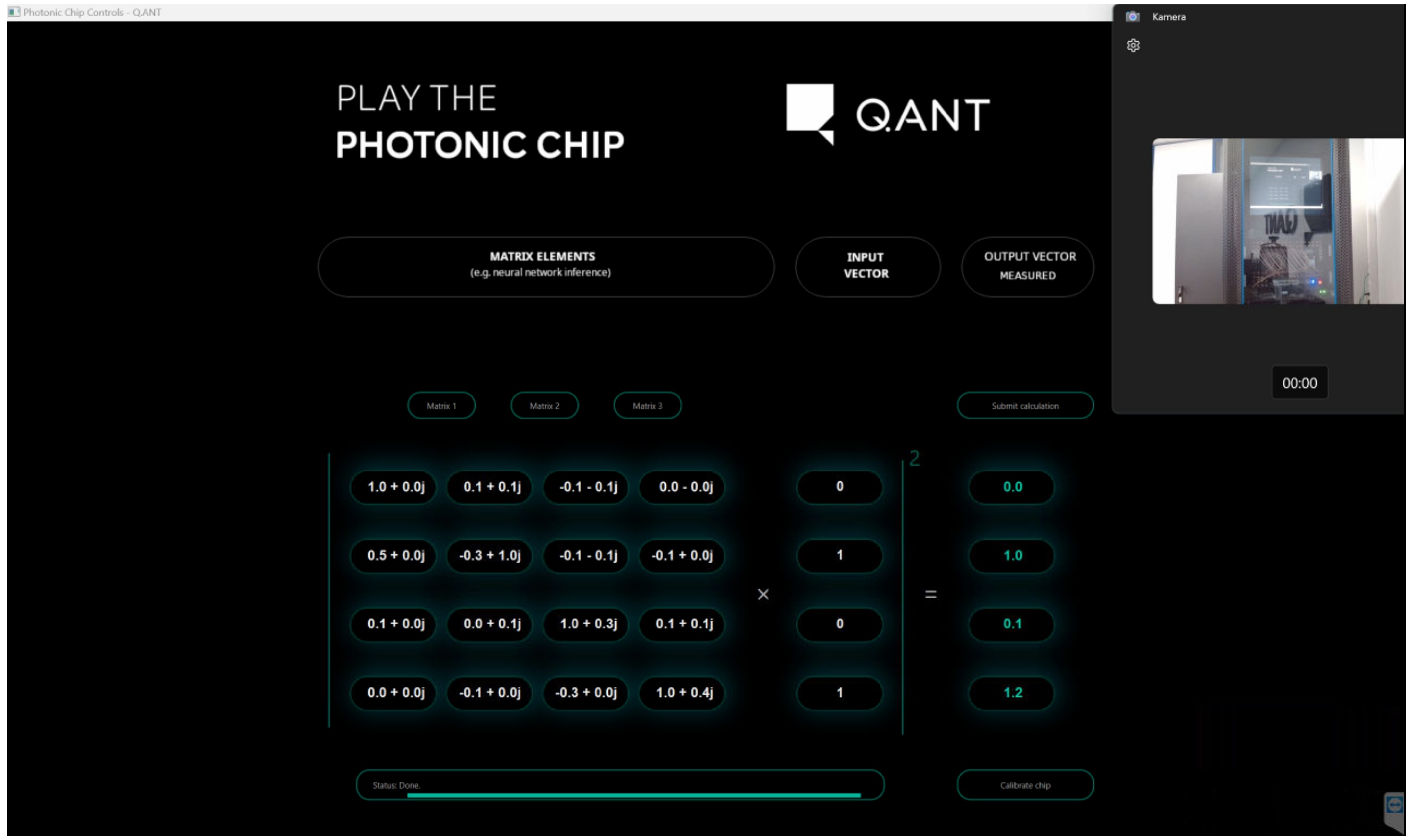
- Scaling to 20 x 20 matrix sizes is ongoing
- Key devices: MZMs with spiral-electrodes and fiber array inputs

Status Jan. 2024: First 4 x 4 processor realized, 20 x 20 chip manufactured

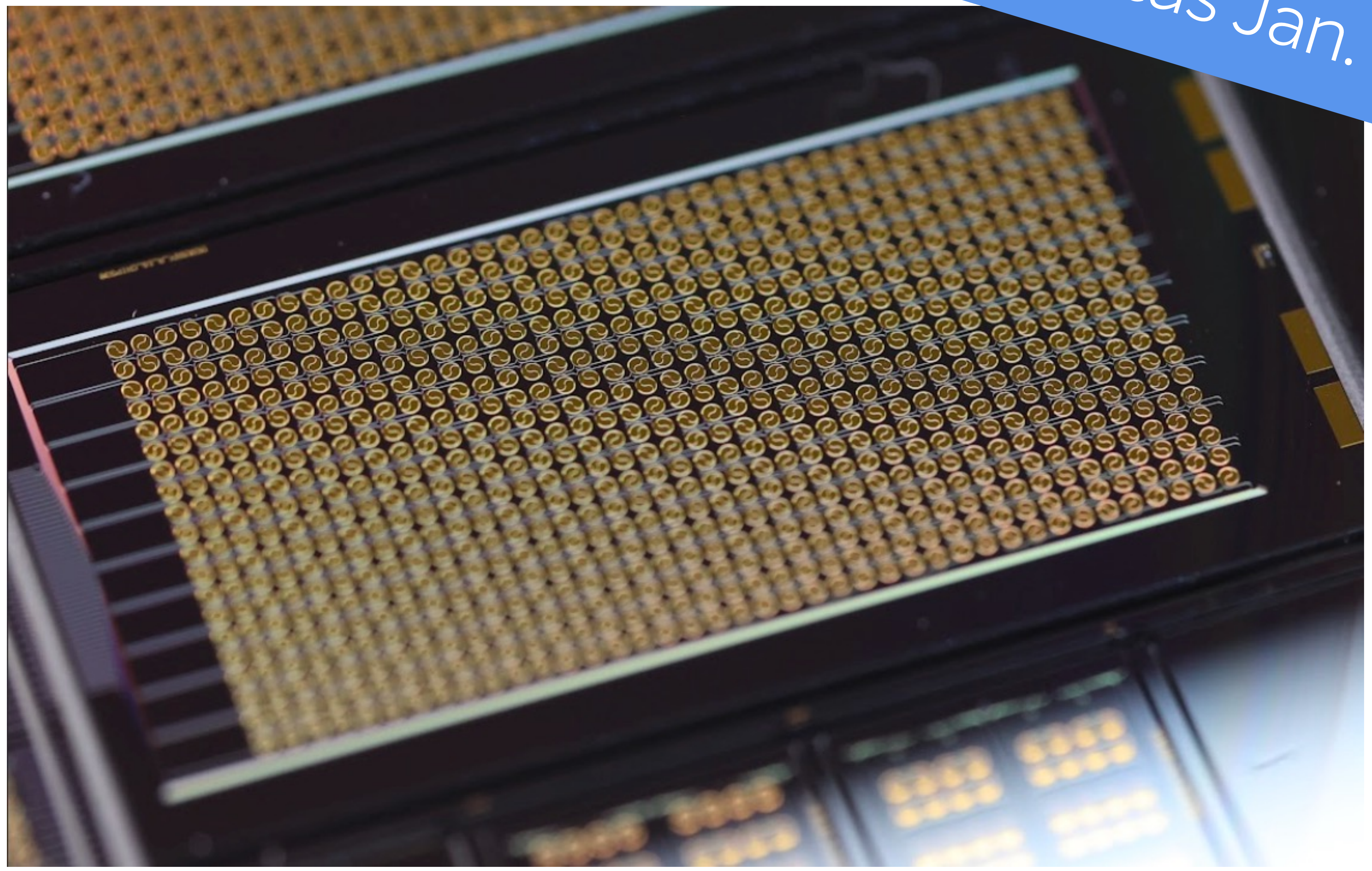
Processor presented at CadenceCONNECT 'Rise of Photonic Computing' (07. Feb. 24)

Status Jan. 2024

First 4 x 4 matrix-vector processor



20 x 20 chip is fabricated



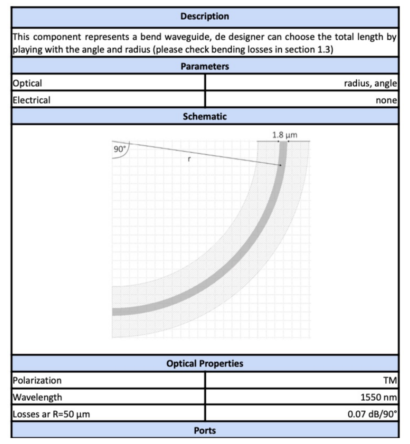
- Clock frequency: 1 MHz
- System power consumption: < 1kW @230V
- Control: 2x5U 19" Rack
- Chip temperature: 22°C
- Ambient temperature: +10°C ≤ T ≤ +40°C
- Availability: 2024

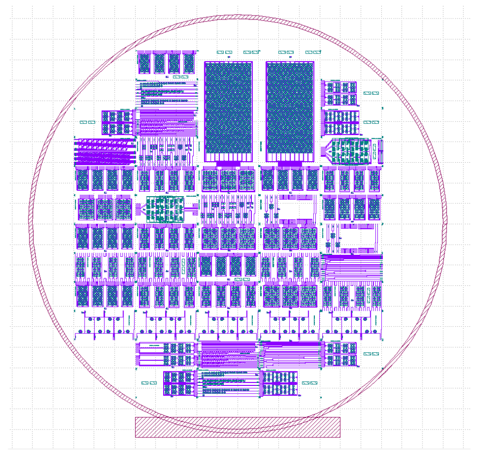
We have developed proprietary processes for TFLN PIC fabrication

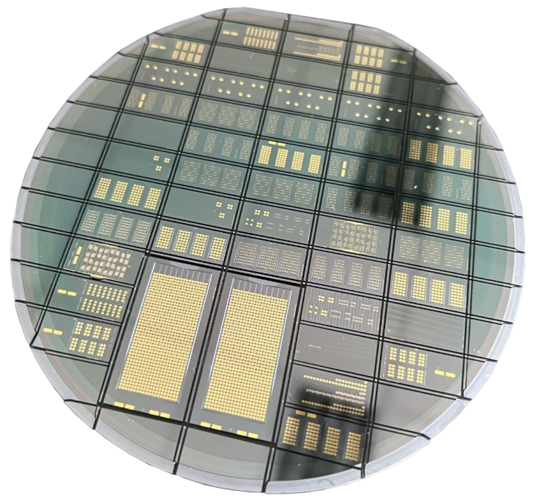
and are now starting to bring everything together into our own pilot line by 2025.

We cover the essential parts of the PIC value chain

We are the only source outside Asia





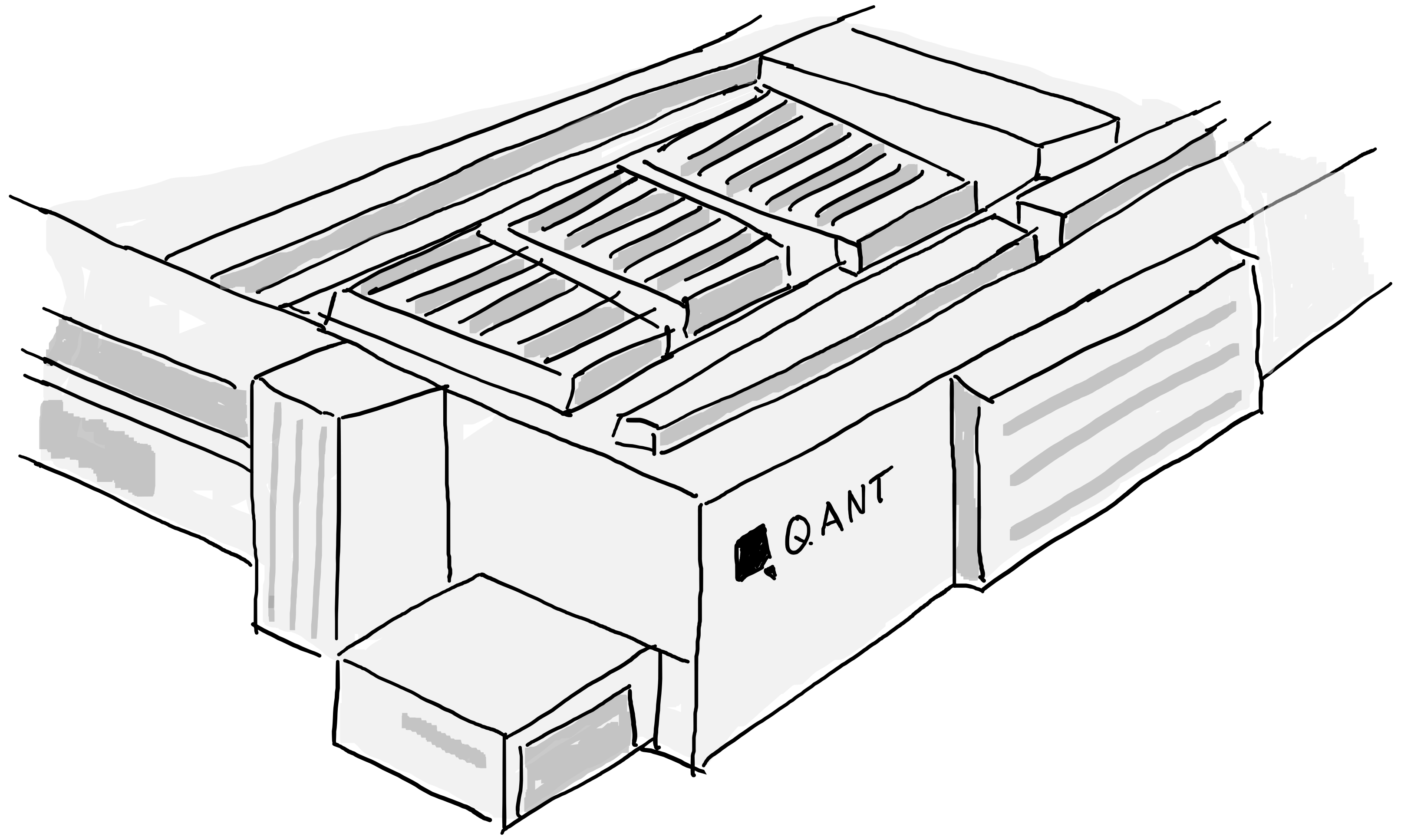


TFLN Wafers fabrication › Designs › Layout & Masks › Fabrication

Fabrication:
- Front End
  - Poling
  - FEoL
  - BEoL
  - Dicing

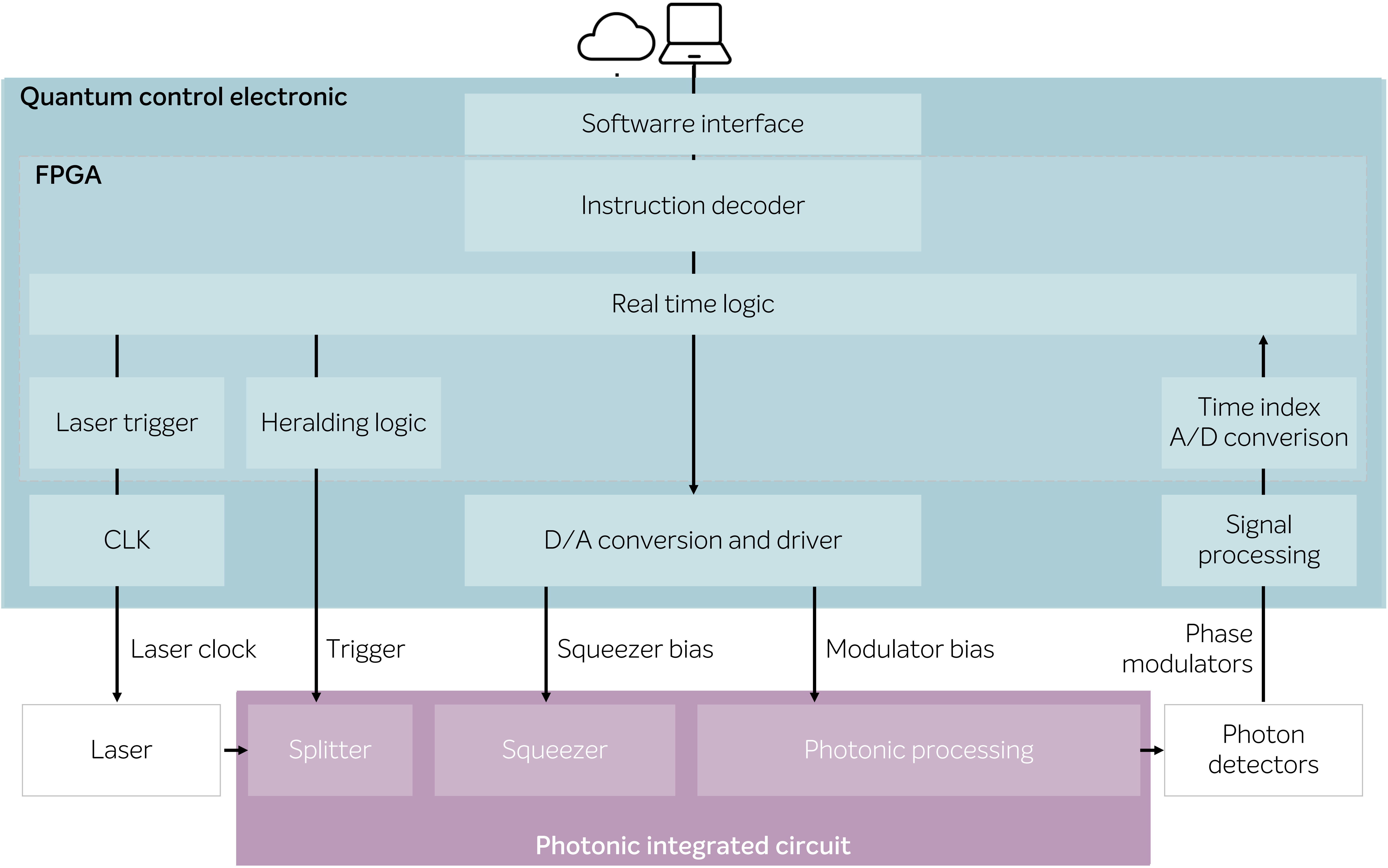
Own pilot fabrication line by 2025

Partnership with IMS Chips



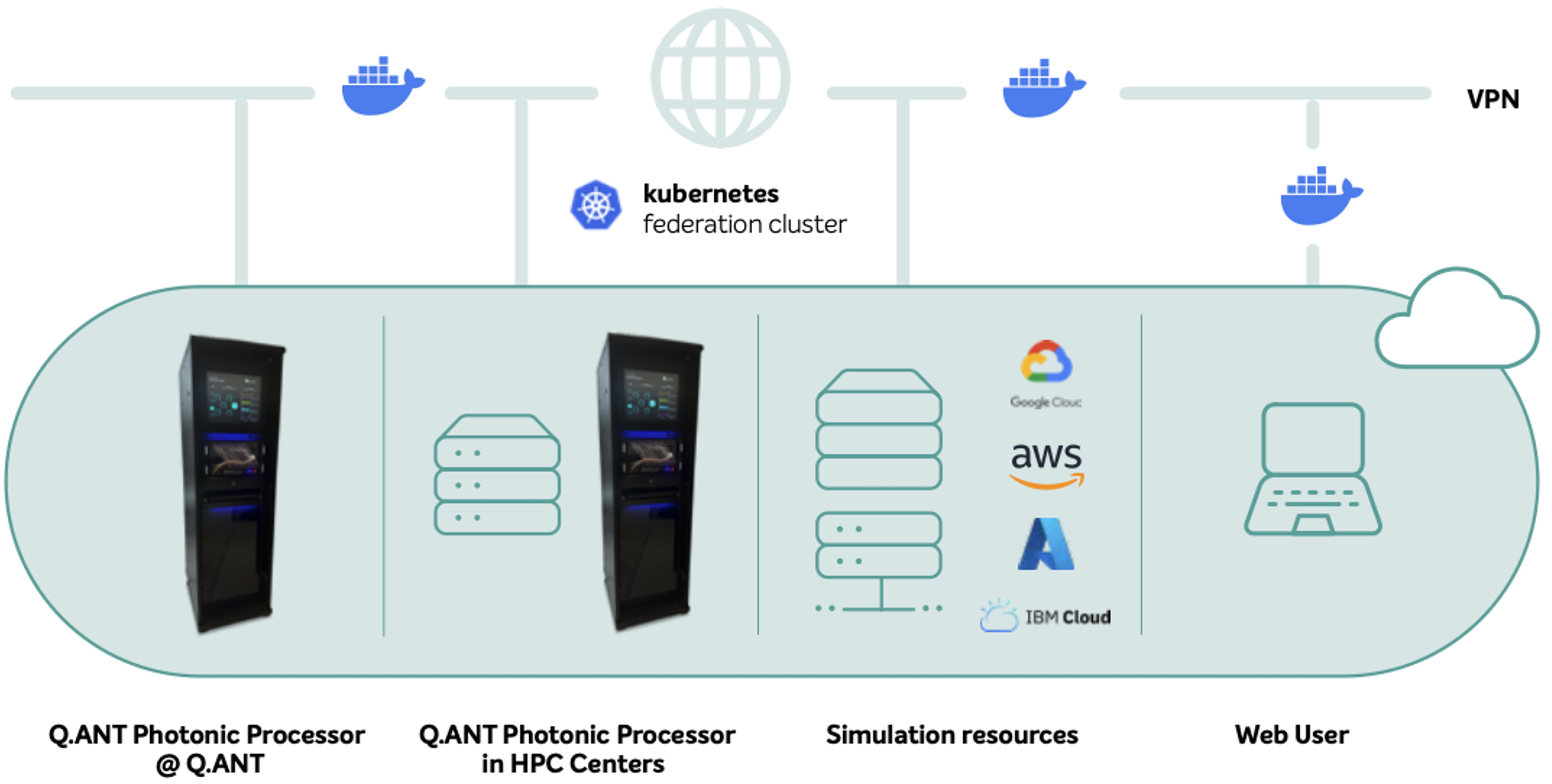
Q.ANT

We deliver the complete photonic processor.

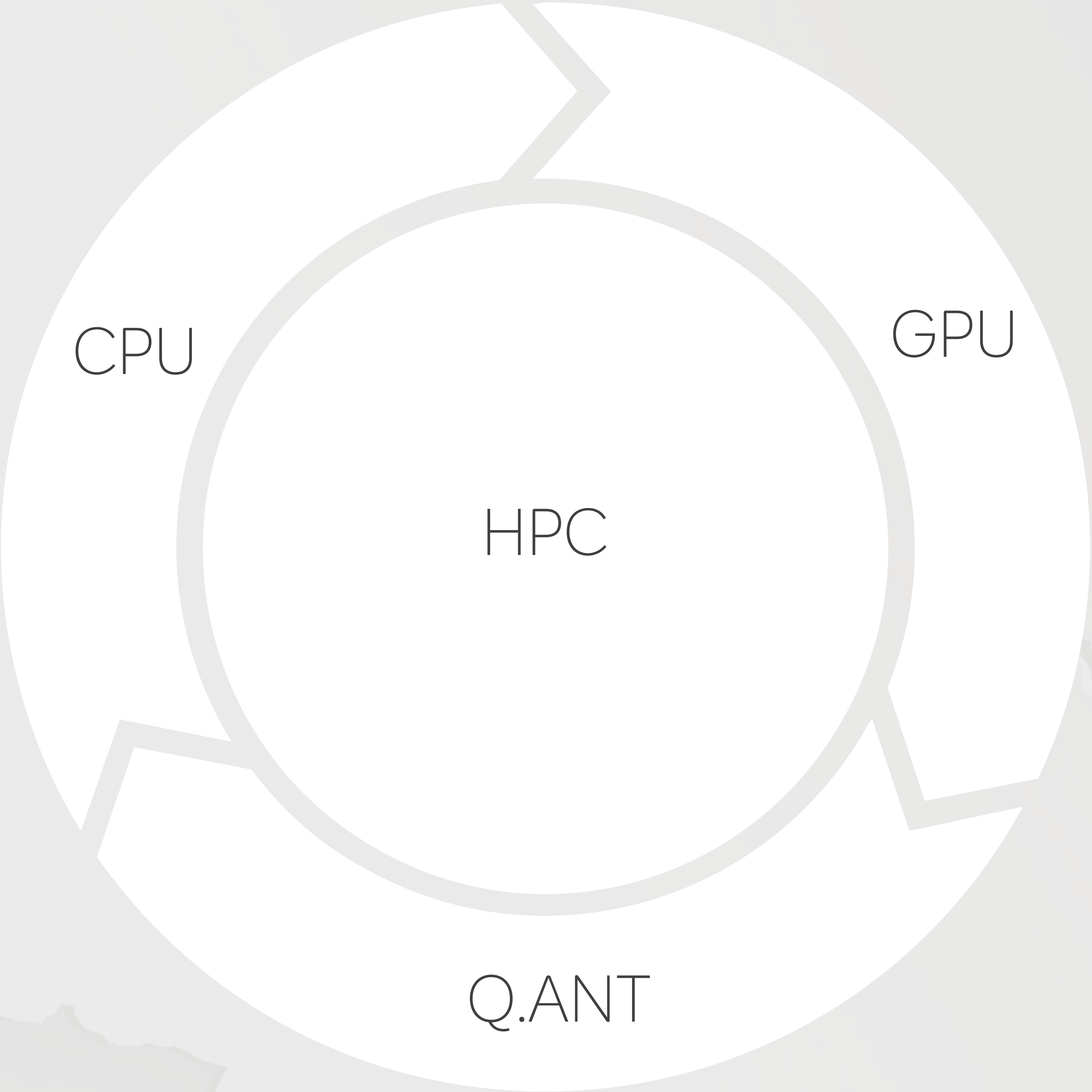


Q.ANT

Our cloud computing infrastructure will provide easy access thanks to the Q.ANT federation cluster.



Q.ANT processers will be part of High Performance Computing Centers



Applications

or how to get a share of the computing industry

Computing has three important figures of merit

Performance, Energy, and Cost

Performance

How fast can you solve a given task

Energy

How much energy is used for the task

Costs

What is the total cost of ownership

State of the art: Nvidea Blackwell B200

5000 TOPS (INT8)

1.200 W per card
0,24 TOP/J

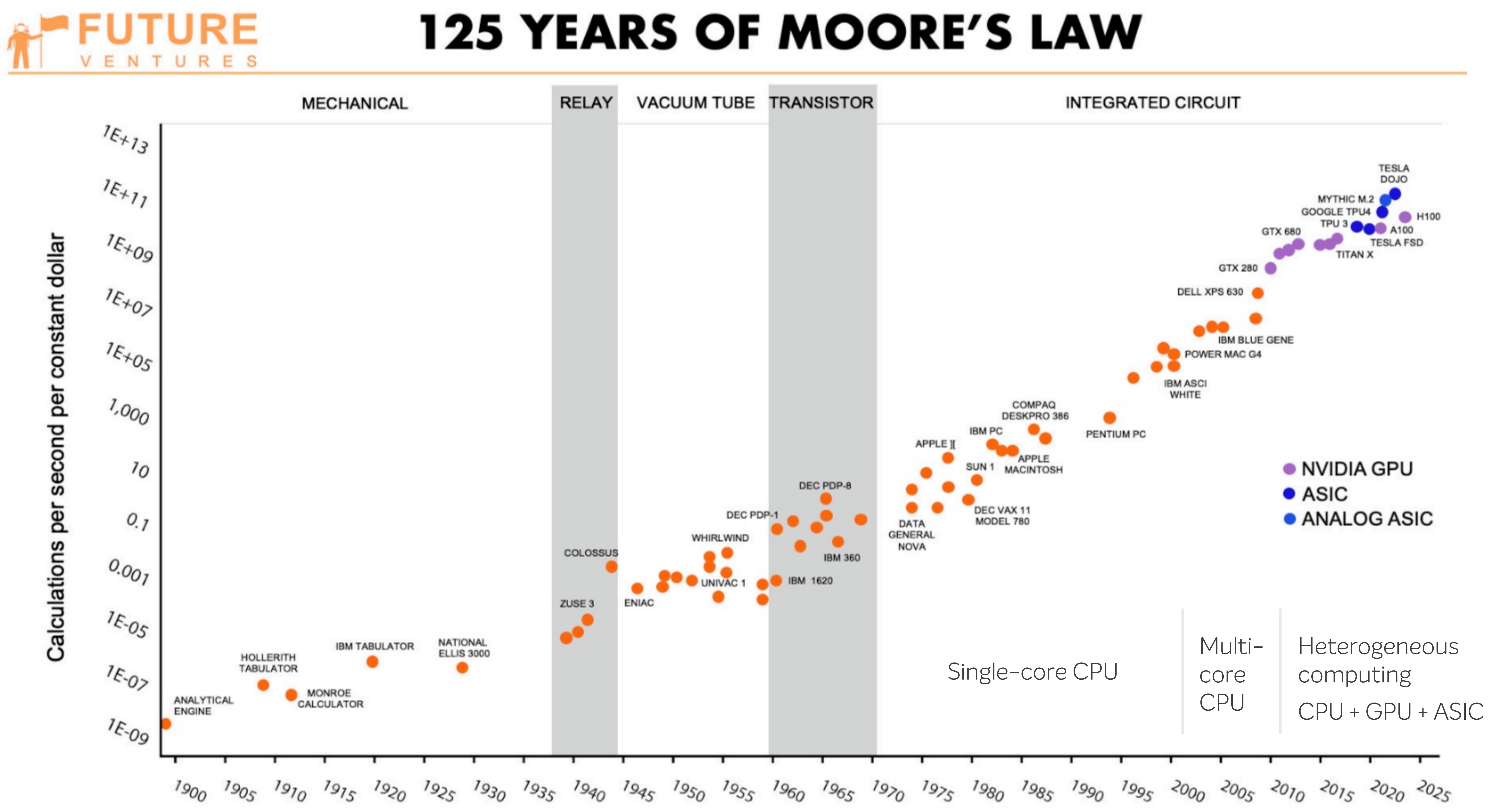
250 $ per untested chip

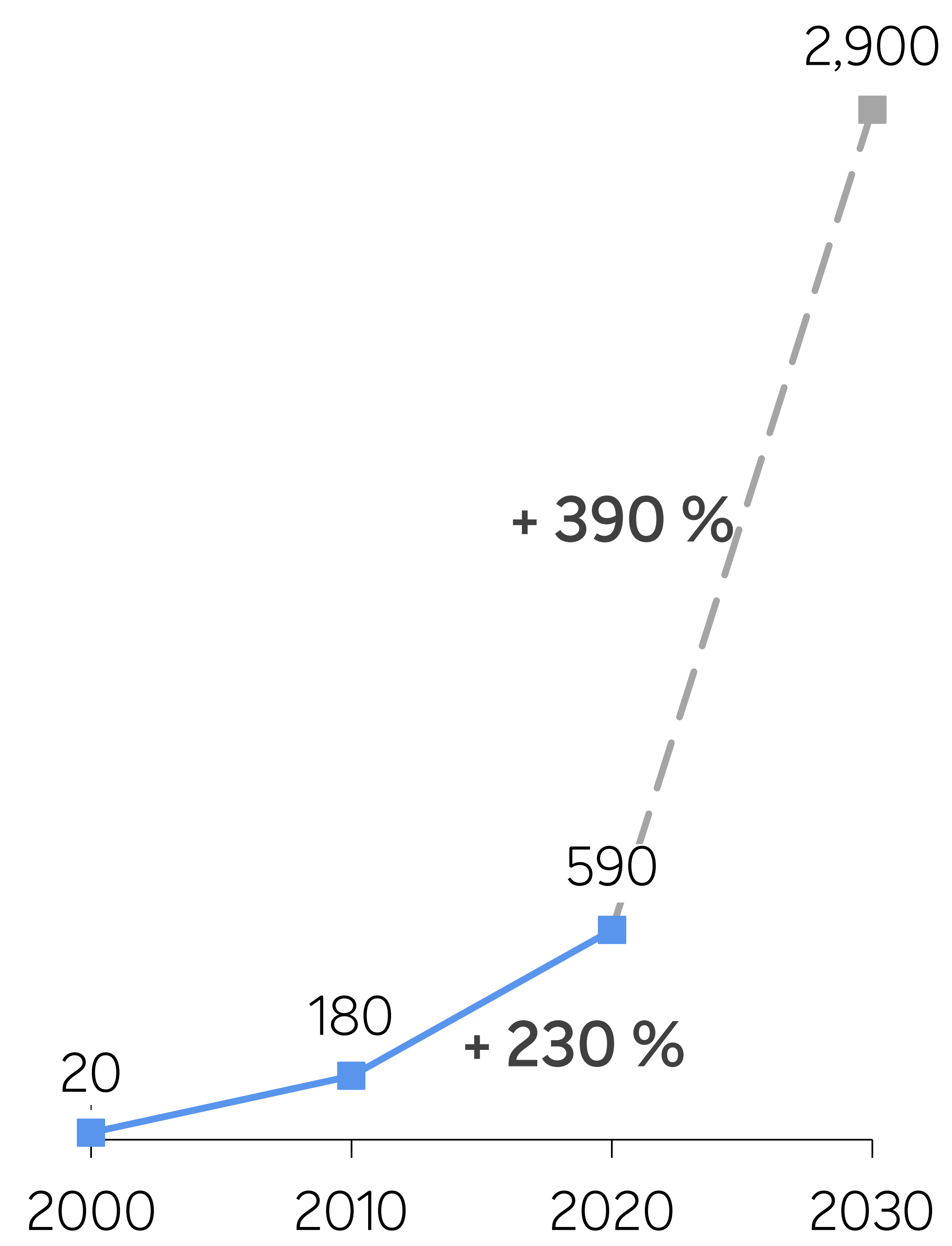
TOPS = Tera Operations per Second // 1 Trillion operations per second
Source: NVIDEA Datasheet, TSMC Fab 18

Q.ANT

AI performance needs grow too fast compared to the hardware speed increase.

This requires additional calculation methods – photonics is supposed to support here.

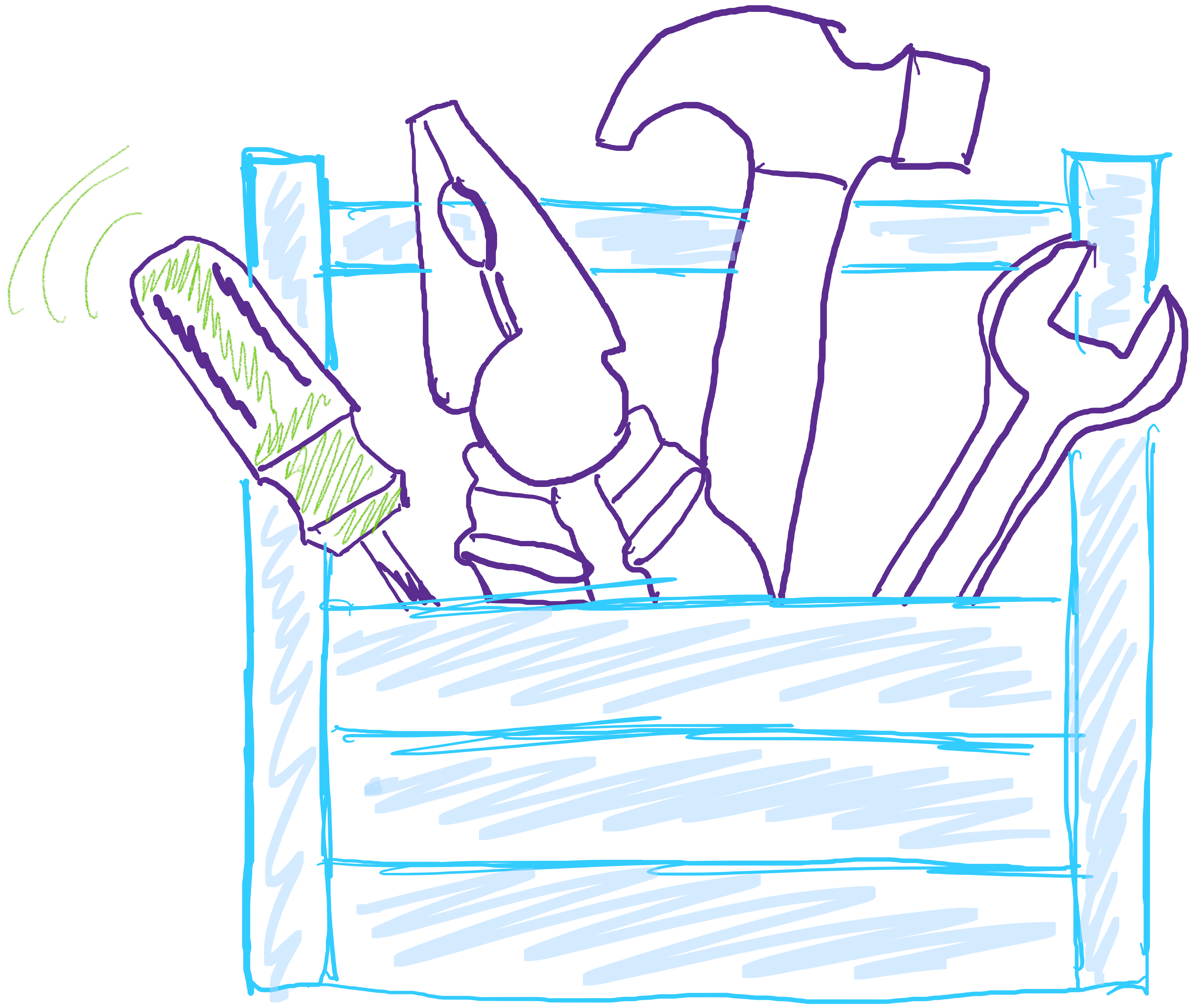




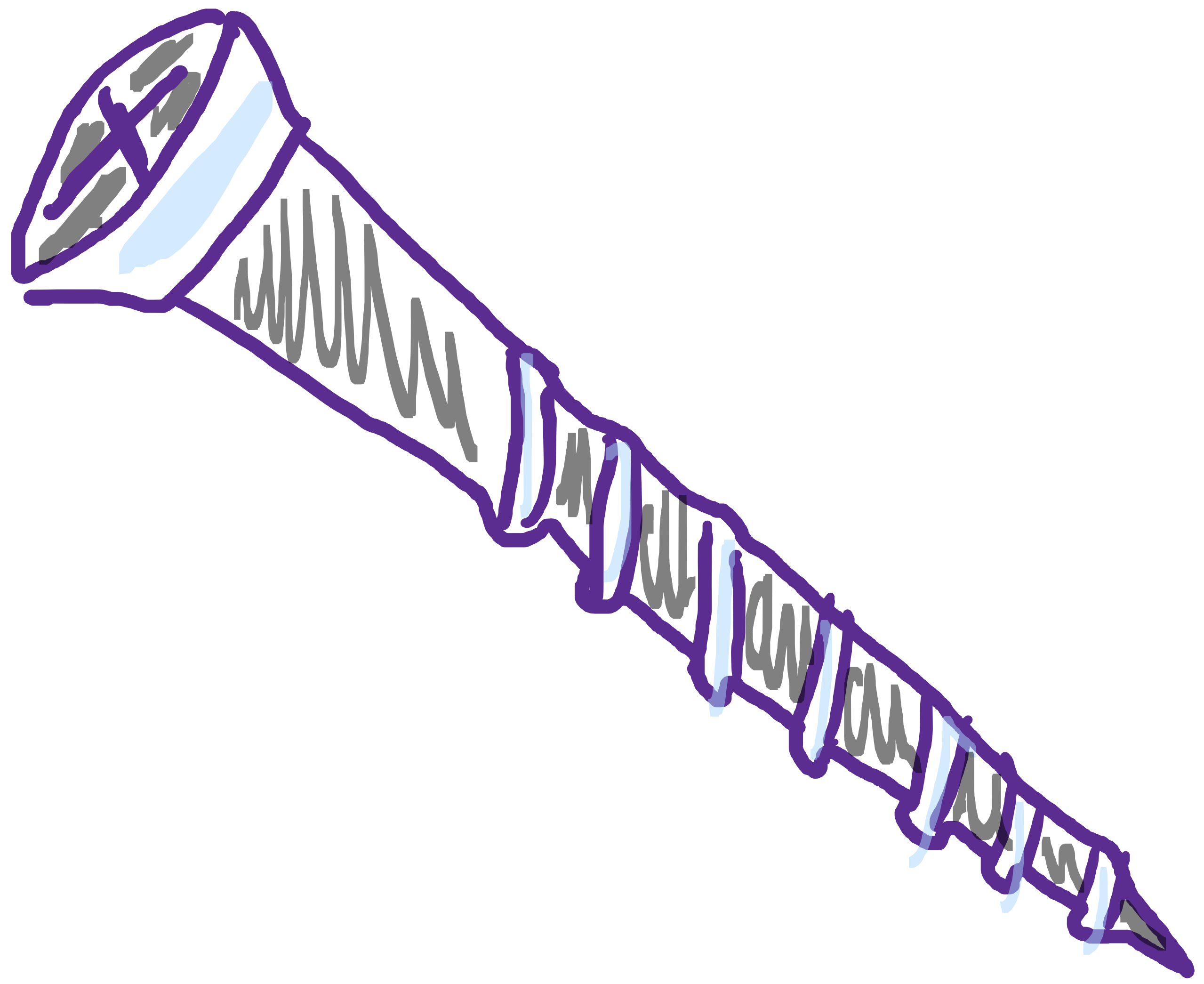
Ray Kurzweil & Steve Jurvetson, adapted from: https://www.reddit.com/r/singularity/comments/paszbd/122_years_of_moores_law_tesla_ai_update/
Katal, A., Dahiya, S. & Choudhury, T. Energy efficiency in cloud computing data center: a survey on hardware technologies. Cluster Comput 25, 675–705 (2022).

The present situation feels like using a hammer to push a screw into the wall.
We must start looking at computing from the problem.

Product offering

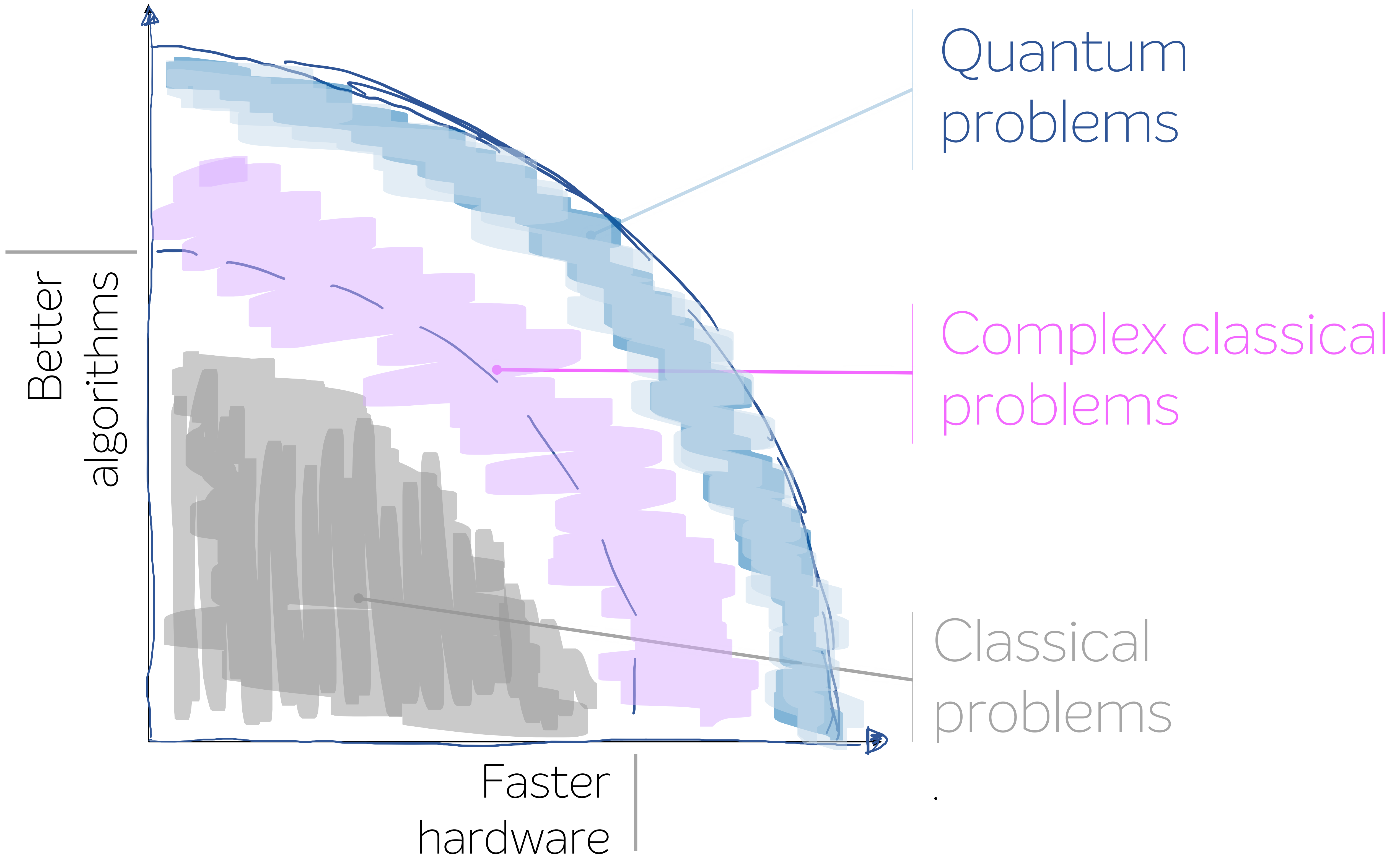


Customer needs

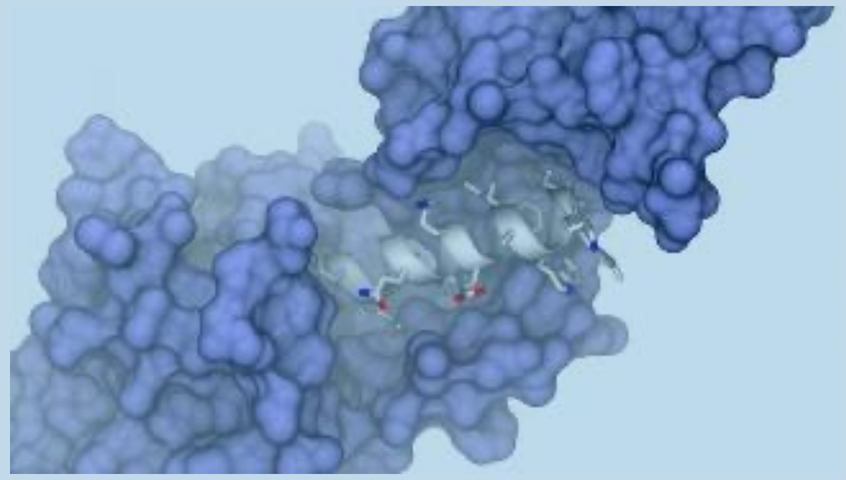


Quantum computing allows the calculation of today's unsolvable problems

which are either genuine quantum problems or complex classical problems.



Example in Drug Discovery:
Determine the electronic structure of the molecule



Picture: ProteinQure

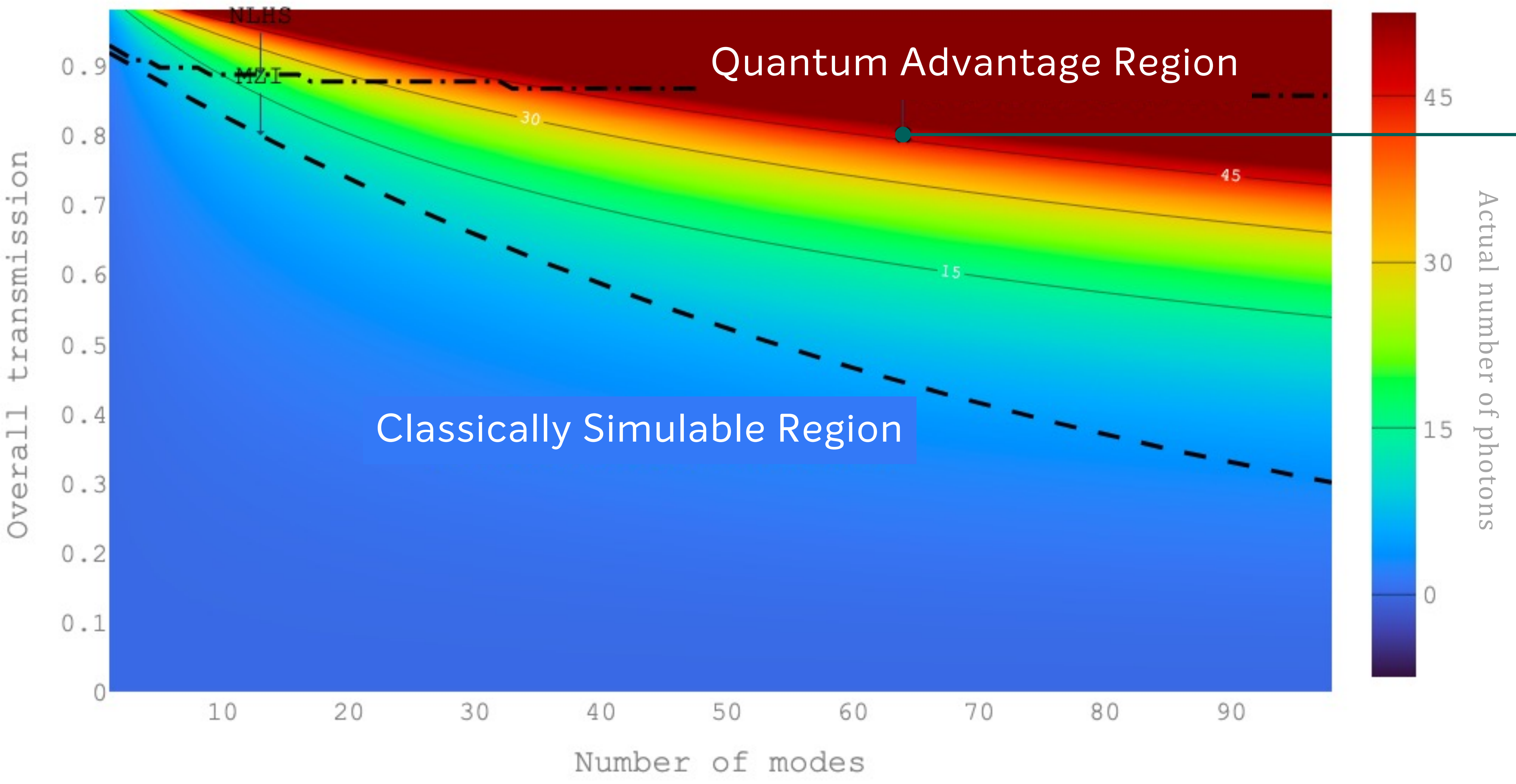
Penicillin molecule has 41 atoms at ground state, modeling the structure requires:

- **Classical computer: 10^{86} bits,** such a machine is a ***physical impossibility***
- **QComputer: 286 logical quantum bits** (Qubits)

Quantum advantage on Gaussian Boson Samplers requires high transmission

which we believe can only achieved in a fully integrated system.

Estimation of quantum advantage of GBS against classical Tensor Network methods



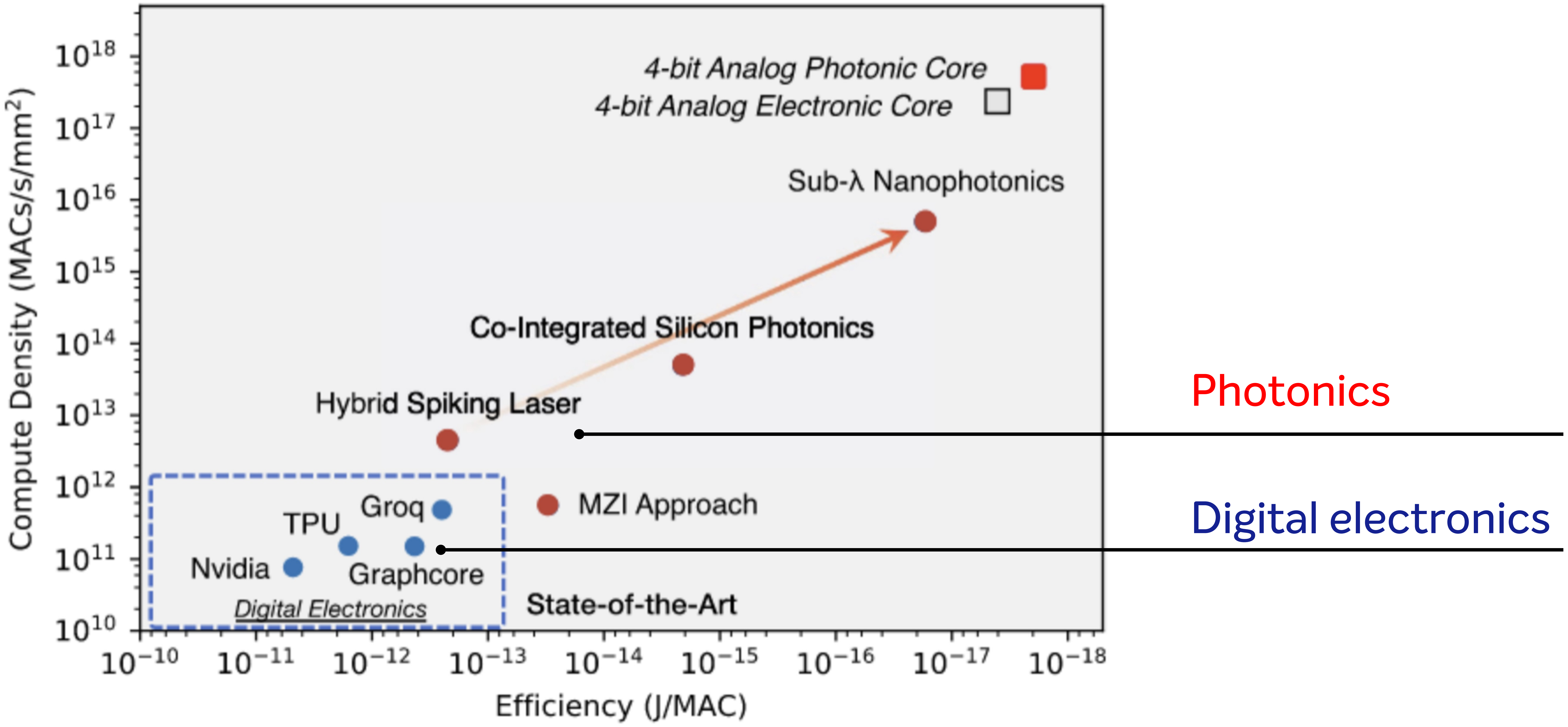
80 % system transmission at 64 modes and 16 dB Squeezing bring us to the edge of quantum advantage

Go, et al. "Exploring Shallow-Depth Boson Sampling: Towards Scalable Quantum Supremacy." arXiv:2306.10671 (2023)
Oh. "Classical algorithm for simulating experimental Gaussian boson sampling." Bulletin of the American Physical Society (2024)

Q.ANT

Photonics can be very efficient in Multiply-Accumulate Operations

compared to state-of-the-art semiconductor AI accelerators



Nahmias et. al, "Photonic Multiply-Accumulate Operations for Neural Networks," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 26 (2020),

Q.ANT

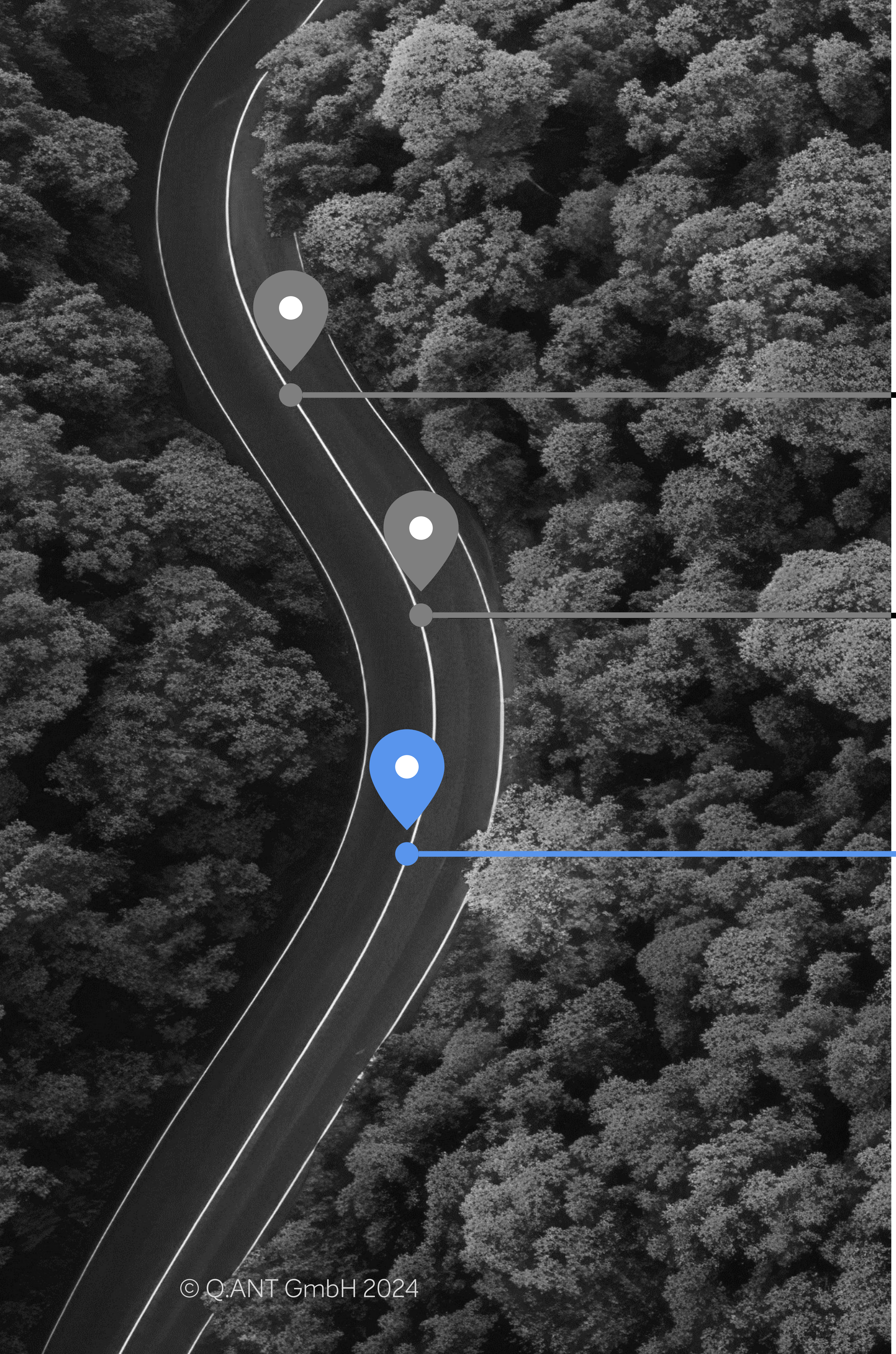
The power consumption is one great advantages of our LNOI chip architecture.

The main power consumers are not on the chip!

Work in progress

System Performance Parameters – preliminary

	Proof-of-concept demo	Matrix vector multiplier (MVM) Generation 1	MVM Generation 2
Release	Feb. 2024	Aug. 2024	2025
DAC Precision	10 bits	12 bits	10 bits
Matrix size	4 x 4	4 x 4	16 x 16
Power consumption	11 W	20 W	150 W
Performance	0.14 OPS	28 MOPS	496 GOPS
Efficiency	80 W / OP	< 700 nW / OP	< 300 pW / OP



Advancements of Para.Digm realizes a roadmap from vector-matrix, to training to Quantum

Processor Three

Quantum

Closed-loop training

Processor Two

Training

Streaming and non-linearities for AI applications

Processor One

Streaming

Vector matrix multiplication for AI acceleration

Stay connected with us:

www.qant.de
start@qant.de

linkedin.com/company/qant
linkedin.com/in/michaelfoertsch/